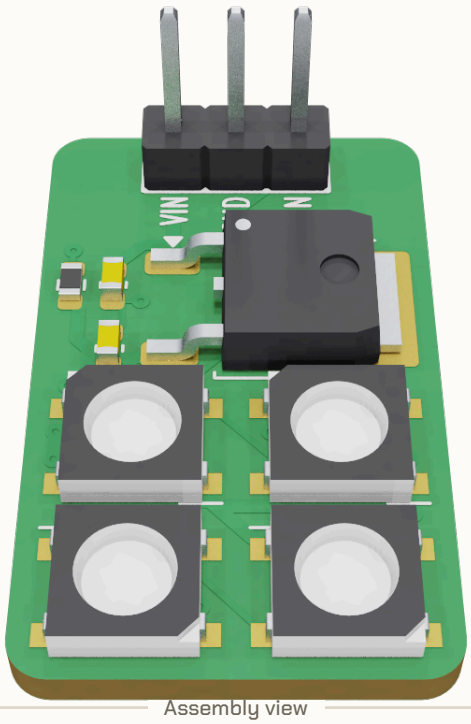
05 Arrays Placement

05-ARRAYS-PLACEMENT - rev A - 2026-10-17 - ENGINEERING RELEASE



Assembly view

Key specifications

Interfaces	host
Outline	15.47 x 25.04 mm
PCB	2 copper layers, 1.60 mm finished thickness
Fitted parts	9

Operating window

VIN supply voltage	`8 V`
VLED supply voltage	`4.749 to 5.251 V`
Ambient operating temperature	`0 to 60 °C`

See Electrical limits for the conditions behind these values, required external loads and contact limits.

Connector overview

CONNECTOR	USE	SIGNALS
J1	host	VIN, GND, DIN

Electrical limits

Operating conditions and limits for the assembled board

Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN	Required input supply voltage	8	—	8	V
VLED supply voltage	VLED	Supply and component tolerances	4.749	—	5.251	V
Ambient operating temperature	TA	Ambient operating range	0	—	60	°C

Electrical characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	IIN	[1, 2, 3, 4]	0	—	167.4	mA
VLED supply current	ILED	[1, 2, 3]	0	—	157.9	mA
Power consumption	P	[5, 4]	—	—	1.34	W

Interface constraints

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
J1 current per contact	I(J1)	Pin 1 [6]	—	—	175	mA
J1 current per contact	I(J1)	Pin 2 [6]	—	—	176	mA
J1 current per contact	I(J1)	Pin 3 [6]	—	—	1	mA

How to use these limits

[1] Maximum instantaneous current in the modeled window, drawn by the board itself.

[2] **Contacts:** What an attachment draws through a connector contact adds to this, up to that contact's limit.

[3] **Tolerances:** Calculated across the listed supply ranges and modeled component tolerances.

[4] **U1 Iq model:** This bound depends on an engineering assumption for this model parameter.

[5] Worst-case input power the board itself draws across all supply rails.

[6] **Contact current:** Each listed pin must not exceed this current. These are application design limits, not connector ratings or available output current.

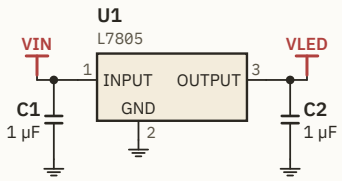
Use only the conditions printed with each value. Component absolute maximum ratings do not automatically apply to the assembled board.

Schematic

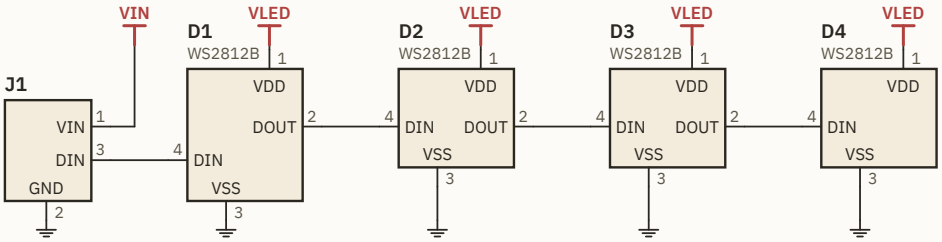
LDO, header, IC, IC, IC and IC and passive network `05-ARRAYS-PLACEMENT`

KEY RAIL IN OUT BIDIR PASSIVE 5·p2 BLOCK 5, PAGE 2

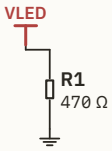
1 LDO L7805



2 Header, IC, IC, IC and IC



3 Passive network

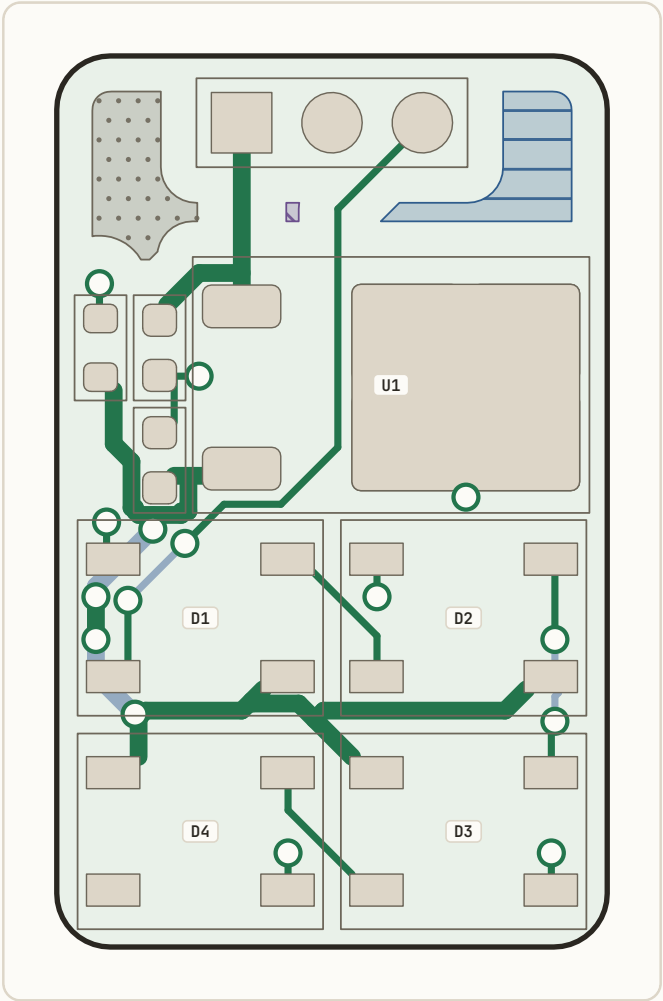


UNUSED PINS NOT SHOWN

Board layout

Copper on both layers, and the board area that no part or track uses

KEY — TOP COPPER — BOTTOM COPPER PAD VIA



TOP VIEW · BOTTOM COPPER SEEN THROUGH · 15 X 25 MM · LARGE PARTS NAMED

Unused area

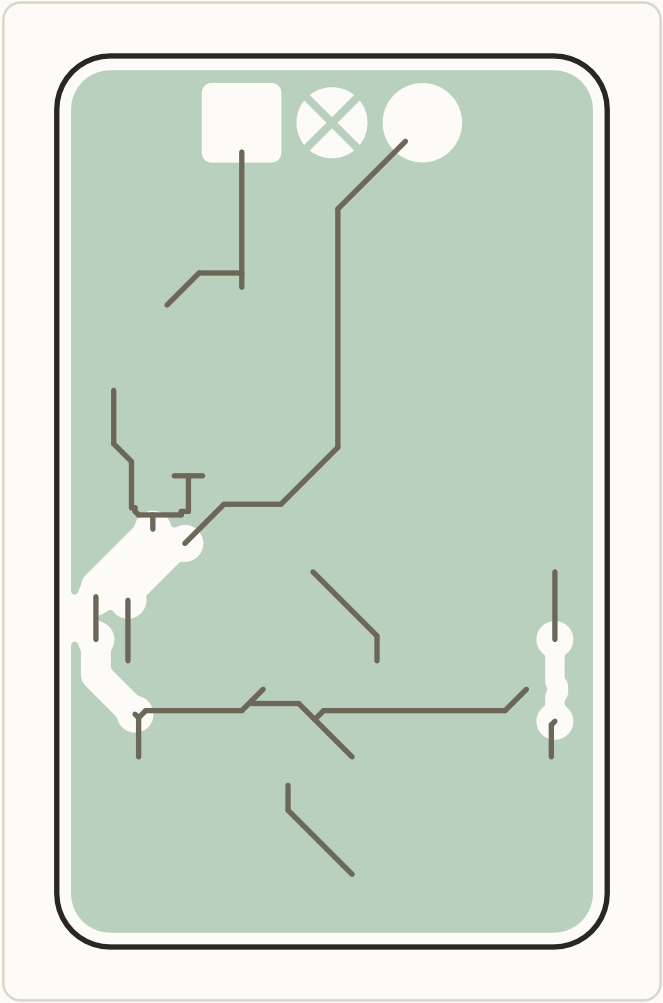
PATTERN	CAUSE	BOUNDED BY	AREA	OF BOARD
	Routing corridor	between tracks	0.2 mm²	0.0 %
	Connector apron	beside a connector	8.8 mm²	2.3 %
	Edge margin	between parts and the outline	9.2 mm²	2.4 %
	Total	at least 1 mm from everything	18.2 mm²	4.7 %

Unused area is board surface at least 1 mm from every part, track and the board edge. A part gap is the only kind a tighter placement can reclaim.

Ground plane

Ground on B.Cu under the routes on F.Cu

KEY GROUND PLANE OPENING ROUTE ON F.CU



TOP VIEW · B.CU UNDER F.CU

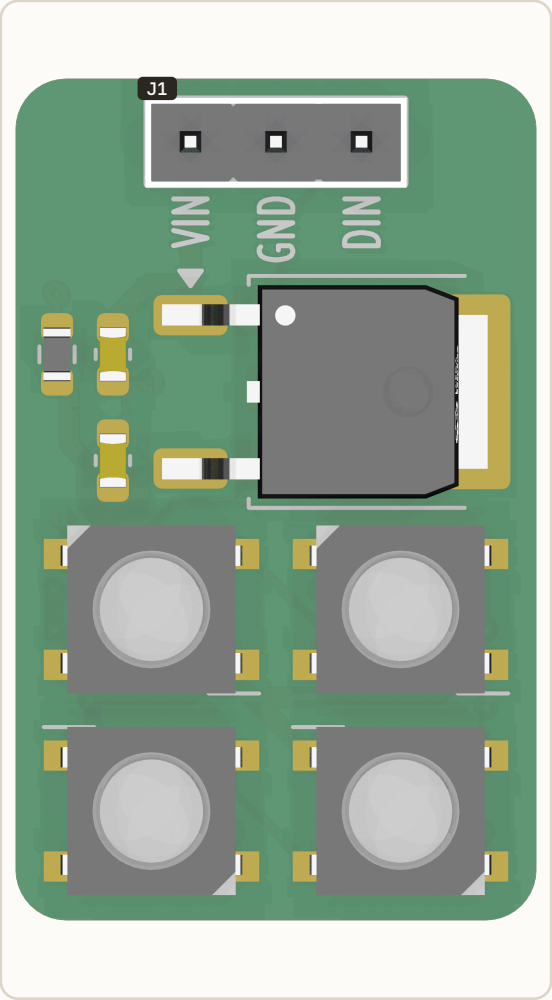
Return path

Ground plane	B.Cu, 86 % of the board
Routes on F.Cu	56 mm; no return detour of 1 mm or more

Openings in the plane add under 1 mm to the return path of a route on F.Cu above them; no route on F.Cu crosses a gap that adds more.

Board connections

Connector and test point locations viewed from the top of the assembled board



TOP VIEW - CONNECTORS AND TEST POINTS MARKED - NOT TO SCALE

Pin schedules and mating-face views are on the following pages.

Connector pinout

Pin numbers are shown as viewed into the mating face

SIGNAL CLASS POWER GROUND SIGNAL

J1 - host



TOP MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	VIN	8 V supply rail
2	GND	Ground reference
3	DIN	DIN signal

Components on this board

Component identities and supplier codes

IDENTIFICATION VIEWS ARE NOT TO SCALE



C310413
L7805
U1 · QTY 1 · LCSC C310413



C2761795
WS2812B
D1, D2, D3, D4 · QTY 4 · LCSC C2761795



C2937625
host
J1 · QTY 1 · LCSC C2937625

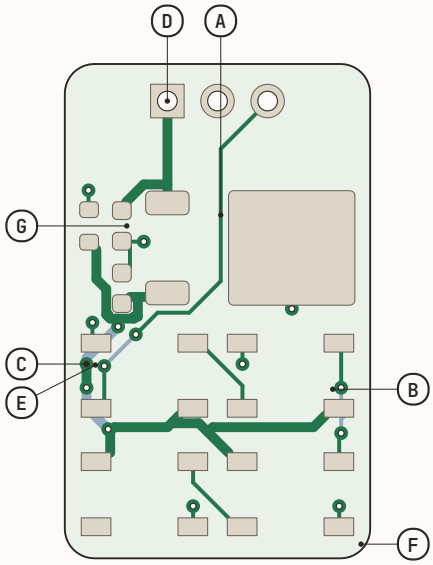
Passives

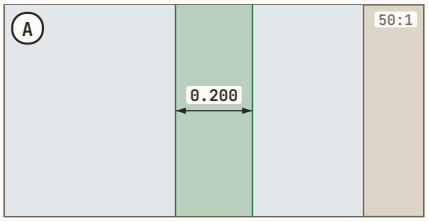
REFERENCE	VALUE / ROLE	QTY	PART
C1, C2	1uF	2	C15849
R1	minimum load	1	C844786

Manufacturability

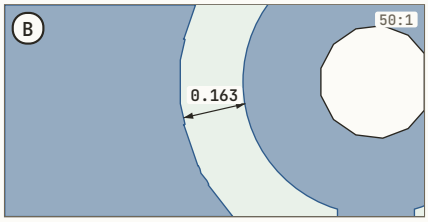
The smallest feature this board asks a fab to make, rule by rule

KEY — TOP COPPER — BOTTOM COPPER — PAD — MASK OPENING

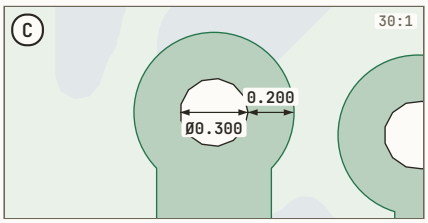




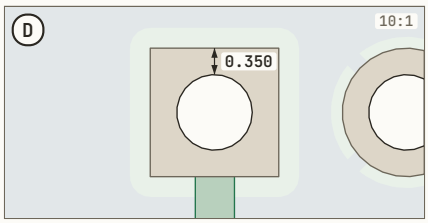
TRACK WIDTH
All 59 track segments
Required minimum 0.200; at minimum



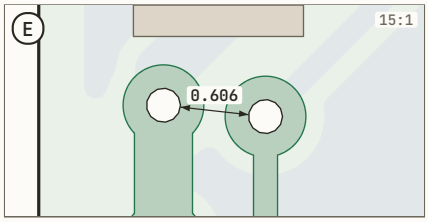
COPPER TO COPPER, OUTER
Every outer gap between nets
Required minimum 0.1524; 0.011 above



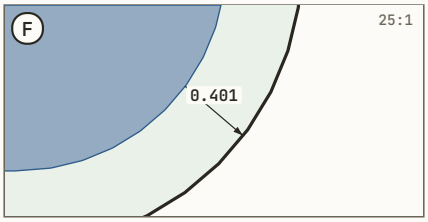
FINISHED DRILL · VIA RING
All 18 holes; all 15 vias
Finished drill minimum 0.300; at minimum.
Via ring minimum 0.200; at minimum



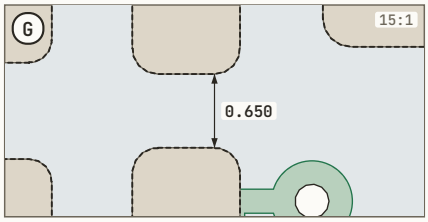
PTH RING
All 3 plated leads
Required minimum 0.300; 0.050 above



HOLE TO HOLE
All 18 holes, wall to wall
Required minimum 0.300; 0.306 above



COPPER TO EDGE
All copper, pours included
Required minimum 0.381; 0.020 above



MASK WEB
All 28 top mask openings
Required minimum 0.1016; 0.548 above

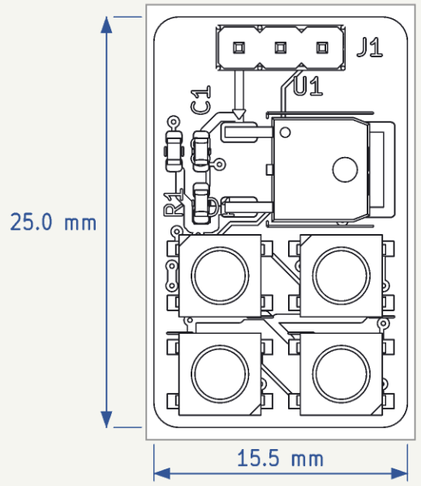
COMPATIBLE FABS

JLCPCB [1] · PCBWay [2] · OSH Park [3] · AISLER [4]

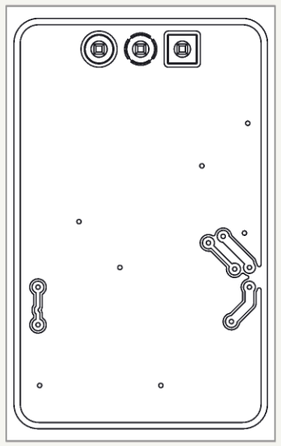
Detail minima use the strictest checked profile. Compatibility means the checked dimensional rules pass.

LAYERS	THICKNESS	ASPECT RATIO	HOLES	DRILL SIZES
2	1.6 mm	5.3 : 1	15 via, 3 PTH	2, Ø0.300–1.000

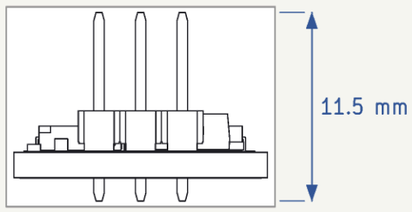
All values in mm. [1] read 2026-08-08 [2] read 2026-08-08 [3] read 2026-08-13 [4] read 2026-08-08



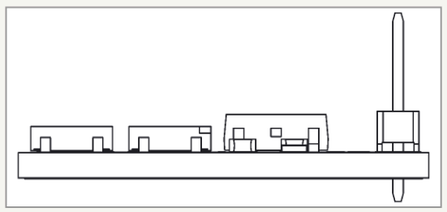
TOP VIEW



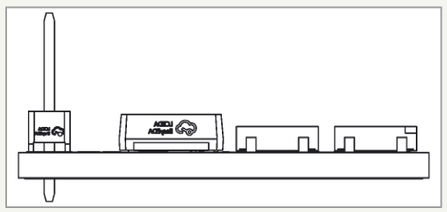
BOTTOM VIEW



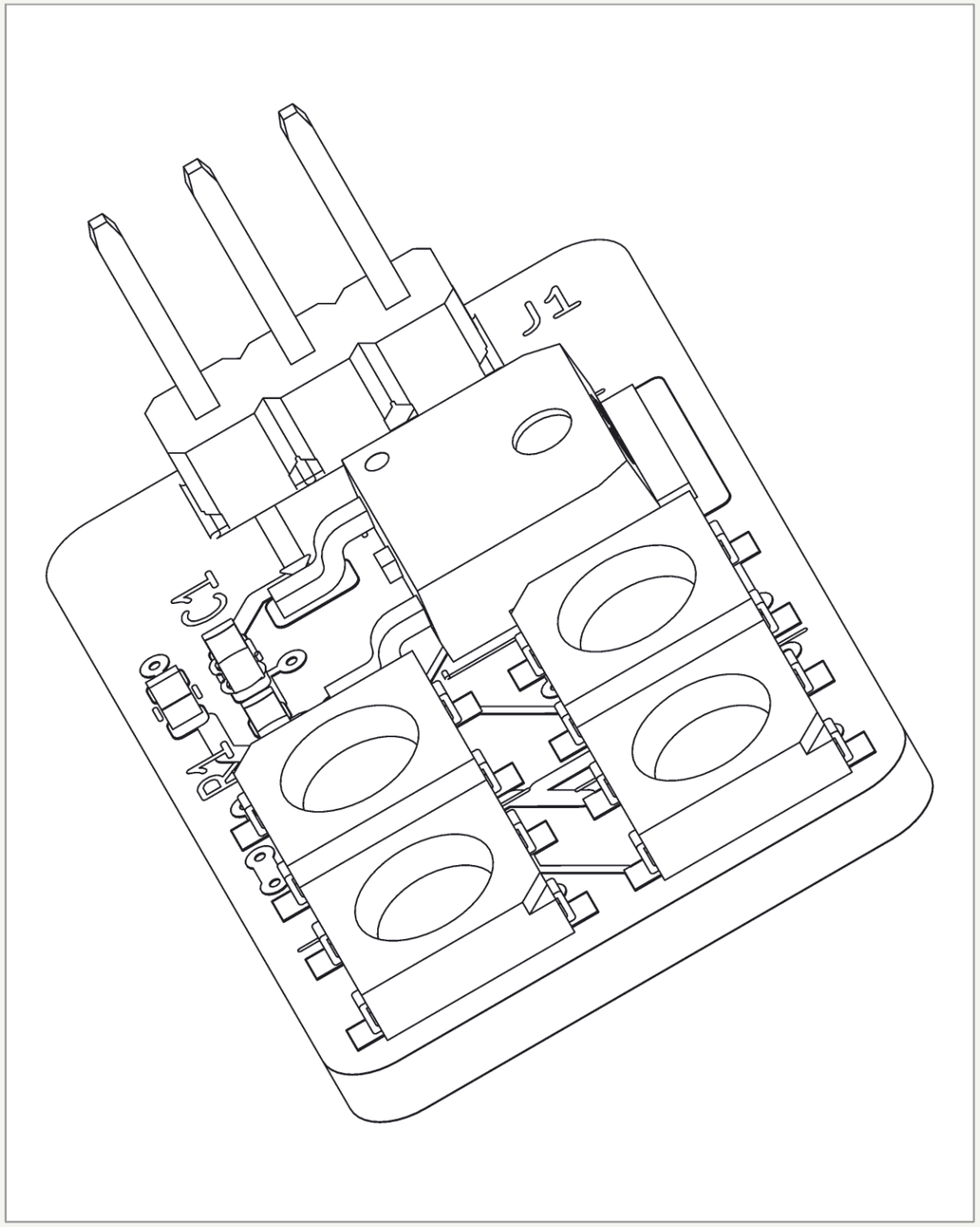
FRONT VIEW (Y)



LEFT VIEW (X)



RIGHT VIEW (X)



ISOMETRIC – NTS

TITLE 05 Arrays Placement assembly	DWG NO. 05-ARRAYS-PLACEMENT
REV A	DATE 2026-10-17
OVERALL 15.5 x 25.0 x 11.5 mm	MATERIAL FR-4, 1.60 mm
PROJECTION REFERENCE VIEWS	SCALE NTS
UNITS mm	SHEET 1 OF 1