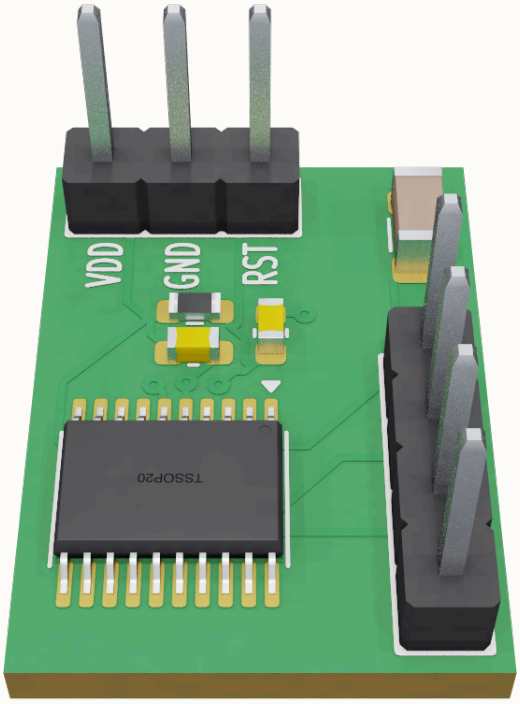
07 MCU Debug

07-MCU-DEBUG - rev A - 2026-10-17 - ENGINEERING RELEASE



Assembly view

Key specifications

Interfaces	power / SWD
Outline	13.95 x 19.01 mm
PCB	2 copper layers, 1.60 mm finished thickness
Fitted parts	7

Operating window

VDD supply voltage	3.3 V
Ambient operating temperature	0 to 70 °C

See Electrical limits for the conditions behind these values, required external loads and contact limits.

Connector overview

CONNECTOR	USE	SIGNALS
J1	power	VDD, GND, NRST
J9	SWD	VDD, SWDIO, SWCLK, GND

Electrical limits

Operating conditions and limits for the assembled board

Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDD supply voltage	VDD	Required input supply voltage	3.3	—	3.3	V
External load impedance	R(J9.1-J9.4)	Between J9.1 and J9.4	99900	—	10010000	ohm
Ambient operating temperature	TA	Ambient operating range	0	—	70	°C

Electrical characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VDD supply current	IDD	[1, 2, 3, 4]	0	—	4.772	mA
Power consumption	P	[5, 4]	—	—	15.76	mW
J9.1 to J9.4 mean-square current	I^2_J9	RMS current squared [6]	—	—	0.00000000109	A^2

Interface constraints

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
J1 current per contact	I(J1)	Pins 1, 2 [7]	—	—	101	mA
J1 current per contact	I(J1)	Pin 3 [7]	—	—	20	mA
J9 current per contact	I(J9)	Pin 1 [7]	—	—	0.033	mA
J9 current per contact	I(J9)	Pins 2, 3 [7]	—	—	20	mA
J9 current per contact	I(J9)	Pin 4 [7]	—	—	101	mA

How to use these limits

[1] Maximum instantaneous current in the modeled window, drawn by the board itself.

[2] **Contacts:** What an attachment draws through a connector contact adds to this, up to that contact's limit.

[3] **Tolerances:** Calculated across the listed supply ranges and modeled component tolerances.

[4] **External loads:** The current and power limits require J9.1 to J9.4: 99900 ohm min, 10010000 ohm max.

[5] Worst-case input power the board itself draws across all supply rails.

[6] **Heating:** Mean-square current is RMS current squared, in A^2. Use it for cycle-averaged resistive heating under the declared steady-waveform model; startup and fault currents need separate limits.

[7] **Contact current:** Each listed pin must not exceed this current. These are application design limits, not connector ratings or available output current.

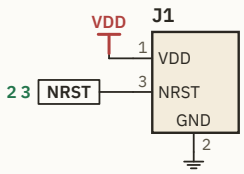
Use only the conditions printed with each value. Component absolute maximum ratings do not automatically apply to the assembled board.

Schematic

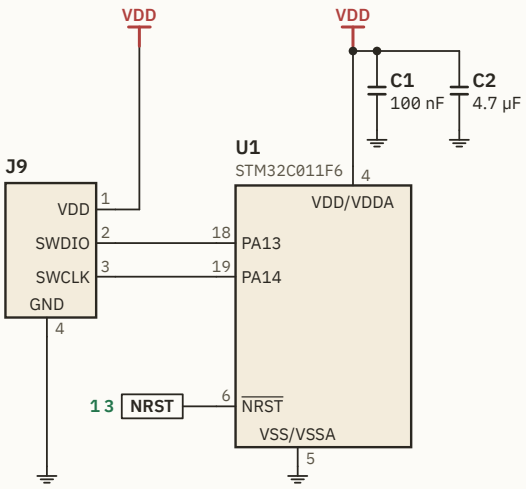
Header, debug header and IC and NRST input 07-MCU-DEBUG

KEY RAIL IN OUT BIDIR PASSIVE 5·p2 BLOCK 5, PAGE 2

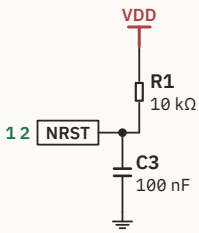
1 Header



2 Debug header and IC STM32C011F6



3 NRST input

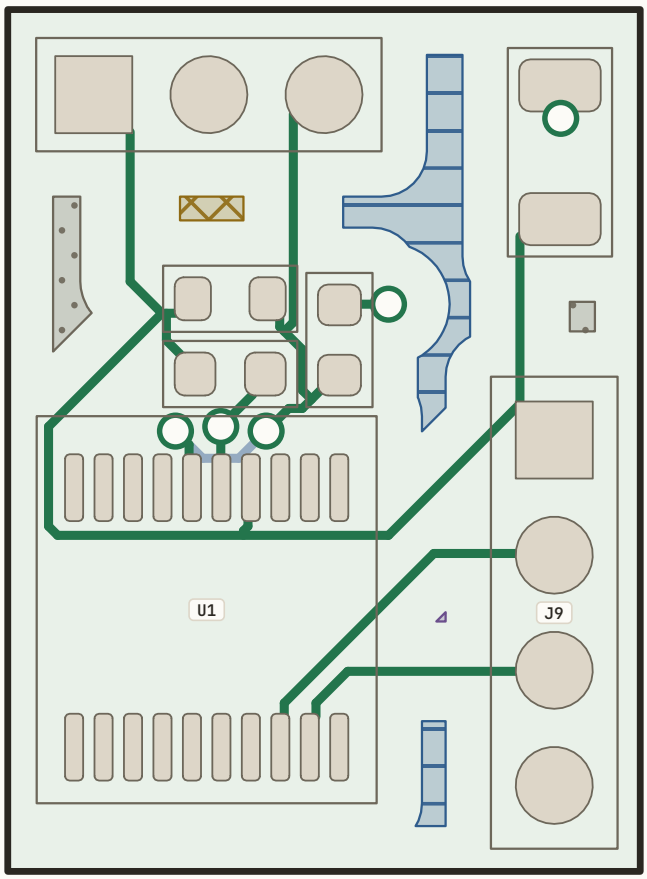


UNUSED PINS NOT SHOWN

Board layout

Copper on both layers, and the board area that no part or track uses

KEY — TOP COPPER — BOTTOM COPPER PAD VIA



TOP VIEW · BOTTOM COPPER SEEN THROUGH · 14 X 19 MM · LARGE PARTS NAMED

Unused area

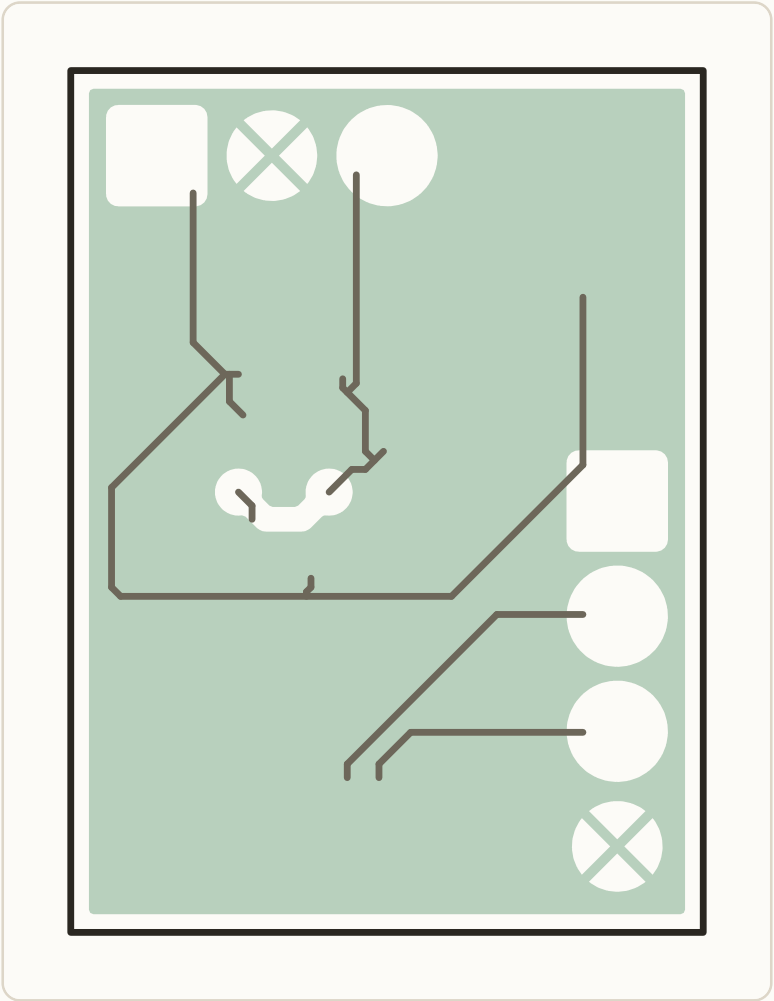
PATTERN	CAUSE	BOUNDED BY	AREA	OF BOARD
	Part gap	between parts	0.7 mm²	0.3 %
	Connector apron	beside a connector	8.6 mm²	3.2 %
	Edge margin	between parts and the outline	2.3 mm²	0.9 %
	Total	at least 1 mm from everything	11.6 mm²	4.4 %

Unused area is board surface at least 1 mm from every part, track and the board edge. A part gap is the only kind a tighter placement can reclaim.

Ground plane

Ground on B.Cu under the routes on F.Cu

KEY GROUND PLANE OPENING ROUTE ON F.CU



TOP VIEW · B.CU UNDER F.CU

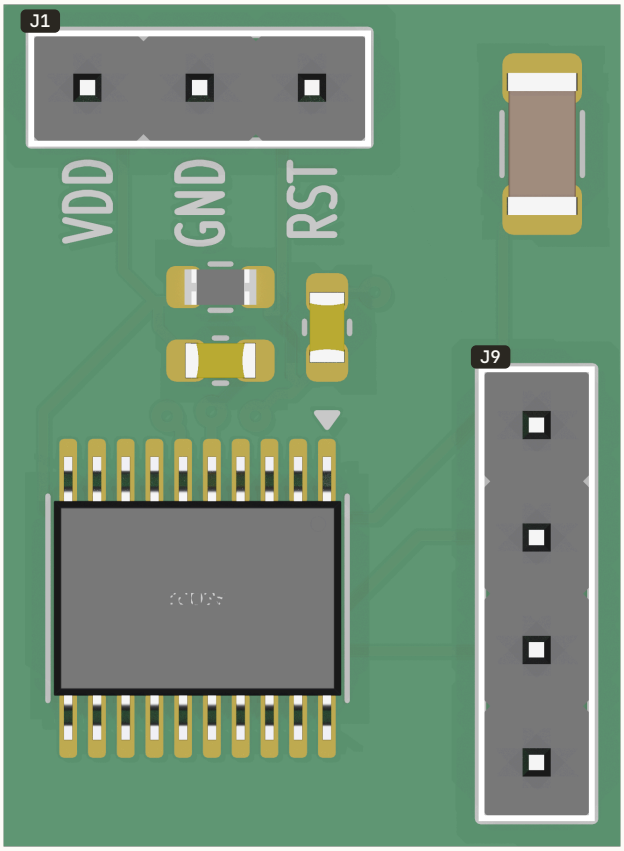
Return path

Ground plane	B.Cu, 79 % of the board
Routes on F.Cu	48 mm; no return detour of 1 mm or more

Openings in the plane add under 1 mm to the return path of a route on F.Cu above them; no route on F.Cu crosses a gap that adds more.

Board connections

Connector and test point locations viewed from the top of the assembled board



TOP VIEW - CONNECTORS AND TEST POINTS MARKED - NOT TO SCALE

Pin schedules and mating-face views are on the following pages.

Connector pinout

Pin numbers are shown as viewed into the mating face

SIGNAL CLASS POWER GROUND SIGNAL

J1 - power



TOP MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	VDD	3.3 V supply rail
2	GND	Ground reference
3	NRST	NRST signal

J9 - SWD



TOP MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	VDD	3.3 V supply rail
2	SWDIO	SWDIO signal
3	SWCLK	SWCLK signal
4	GND	Ground reference

Components on this board

Component identities and supplier codes

IDENTIFICATION VIEWS ARE NOT TO SCALE



C2691448
SWD
J9 · QTY 1 · LCSC C2691448



C2937625
power
J1 · QTY 1 · LCSC C2937625



C5456198
STM32C011F6
U1 · QTY 1 · LCSC C5456198

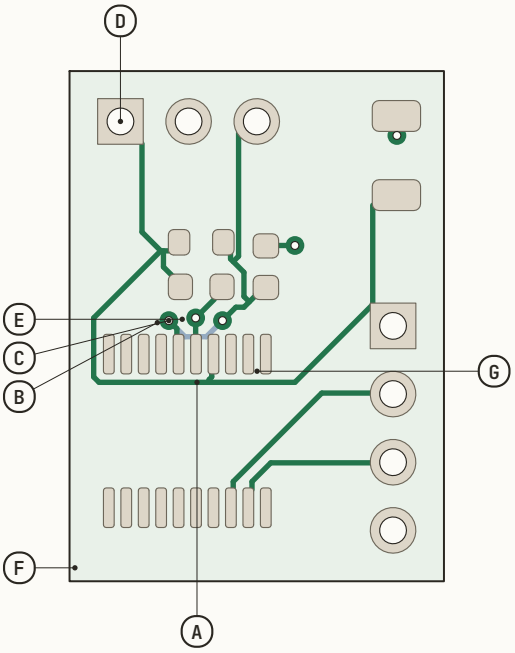
Passives

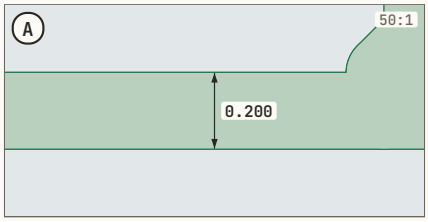
REFERENCE	VALUE / ROLE	QTY	PART
C1, C3	100nF	2	C14663
C2	VDD bulk	1	C440156
R1	10k	1	C844918

Manufacturability

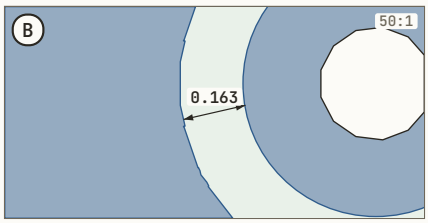
The smallest feature this board asks a fab to make, rule by rule

KEY — TOP COPPER — BOTTOM COPPER — PAD — MASK OPENING

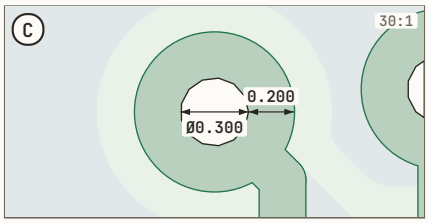




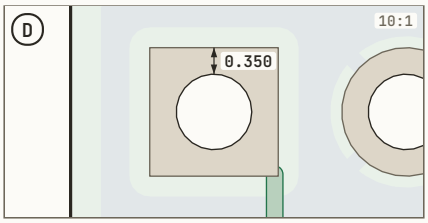
TRACK WIDTH
All 38 track segments
Required minimum 0.200; at minimum



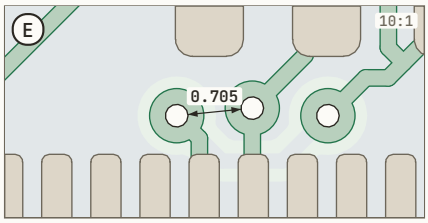
COPPER TO COPPER, OUTER
Every outer gap between nets
Required minimum 0.1524; 0.011 above



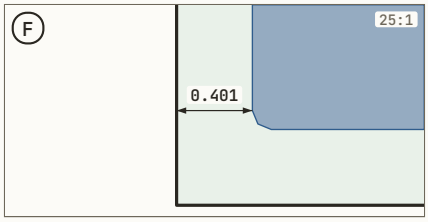
FINISHED DRILL · VIA RING
All 12 holes; all 5 vias
Finished drill minimum 0.300; at minimum.
Via ring minimum 0.200; at minimum



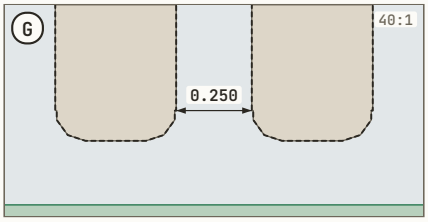
PTH RING
All 7 plated leads
Required minimum 0.300; 0.050 above



HOLE TO HOLE
All 12 holes, wall to wall
Required minimum 0.300; 0.405 above



COPPER TO EDGE
All copper, pours included
Required minimum 0.381; 0.020 above



MASK WEB
All 35 top mask openings
Required minimum 0.1016; 0.148 above

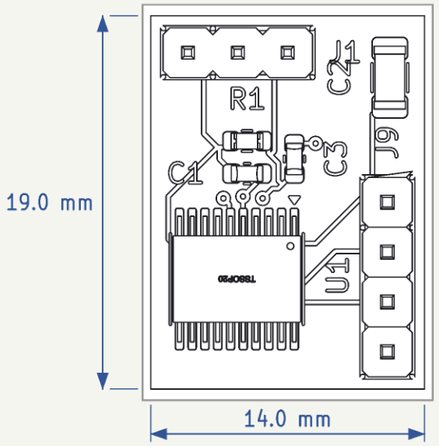
COMPATIBLE FABS

JLCPCB [1] · PCBWay [2] · OSH Park [3] · AISLER [4]

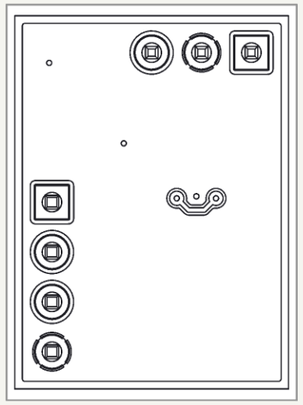
Detail minima use the strictest checked profile. Compatibility means the checked dimensional rules pass.

LAYERS	THICKNESS	ASPECT RATIO	HOLES	DRILL SIZES
2	1.6 mm	5.3 : 1	5 via, 7 PTH	2, Ø0.300–1.000

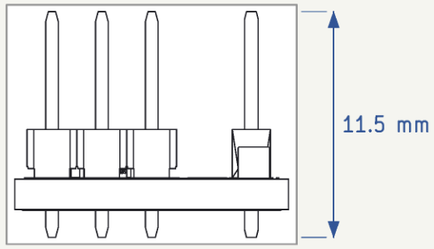
All values in mm. [1] read 2026-08-08 [2] read 2026-08-08 [3] read 2026-08-13 [4] read 2026-08-08



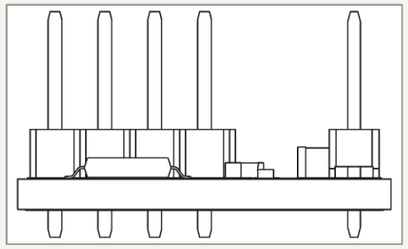
TOP VIEW



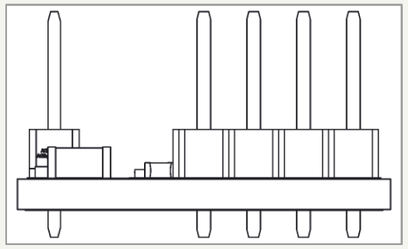
BOTTOM VIEW



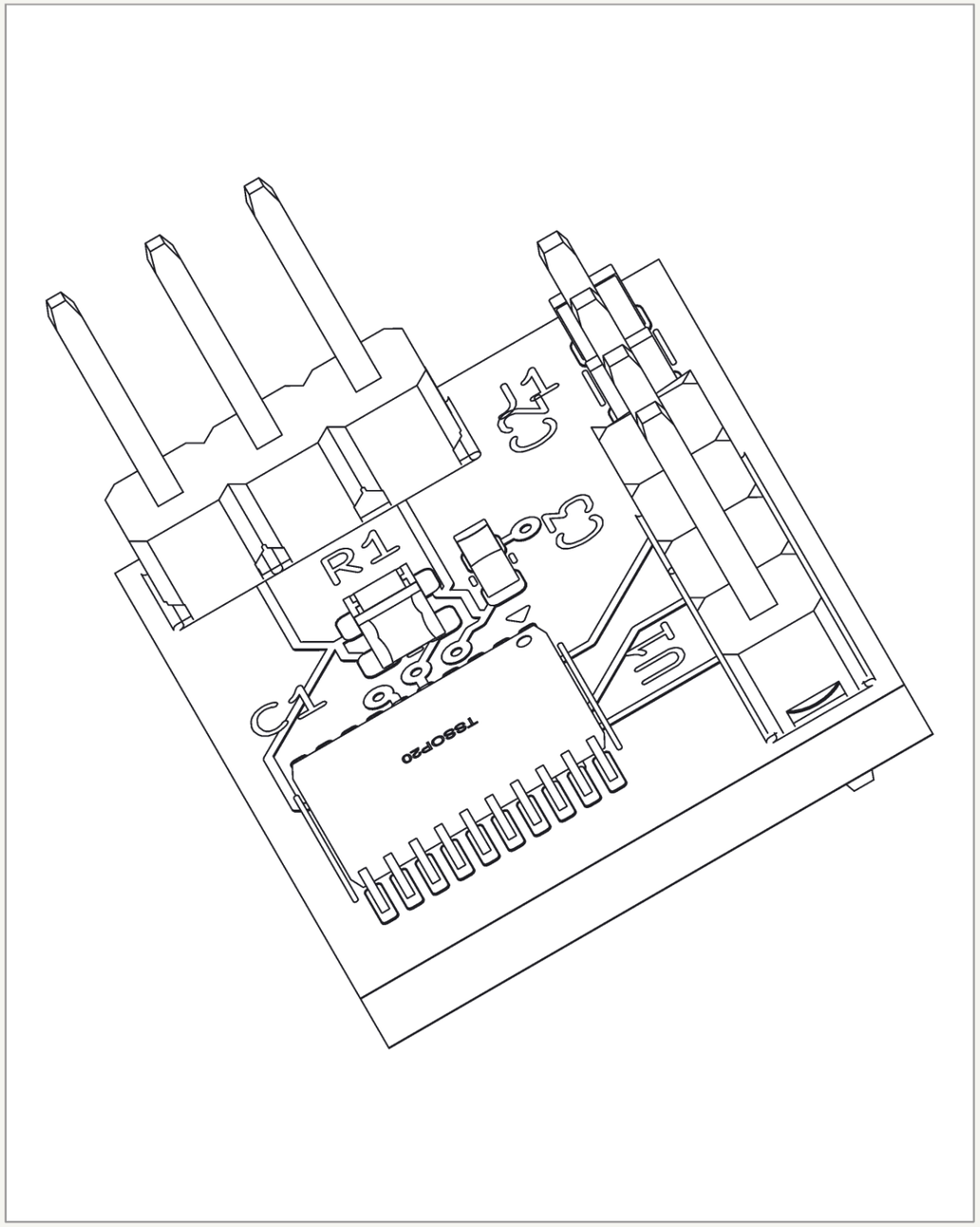
FRONT VIEW (Y)



LEFT VIEW (X)



RIGHT VIEW (X)



ISOMETRIC – NTS

TITLE 07 MCU Debug assembly	DWG NO. 07–MCU–DEBUG
REV A	DATE 2026–10–17
OVERALL 14.0 x 19.0 x 11.5 mm	MATERIAL FR–4, 1.60 mm
PROJECTION REFERENCE VIEWS	SCALE NTS
UNITS mm	SHEET 1 OF 1