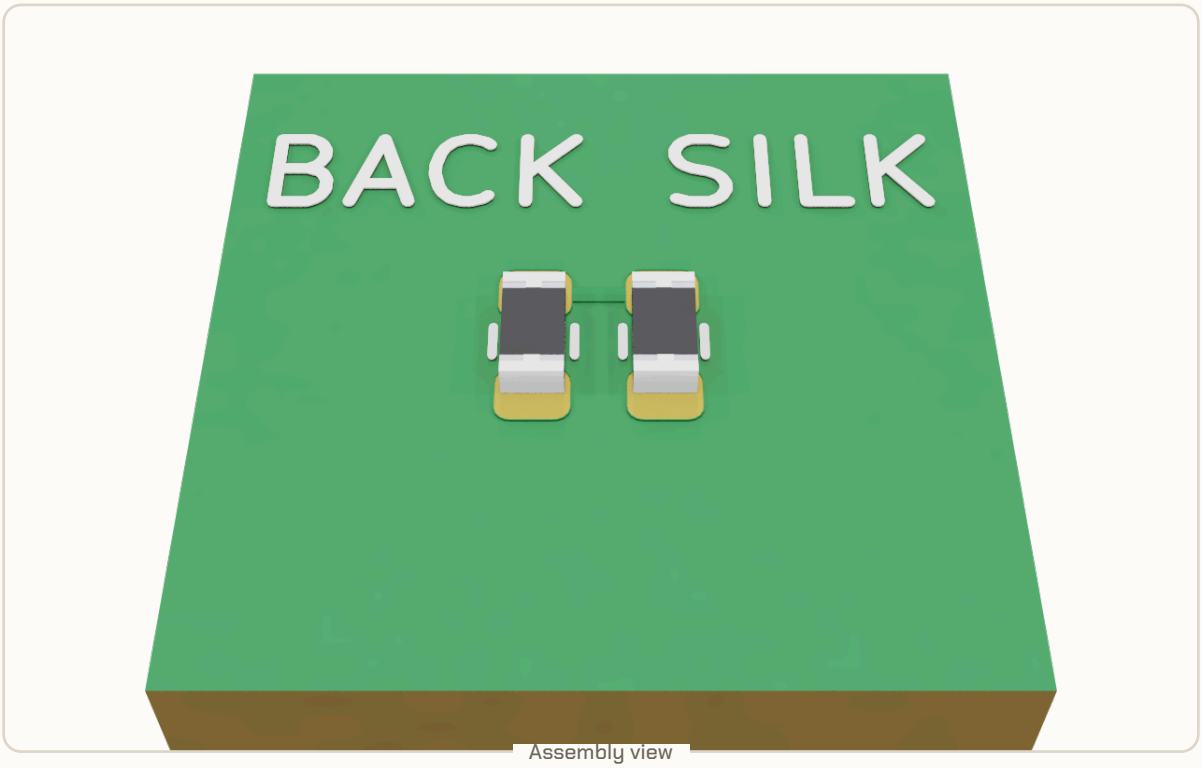
10 Back Silk

10-BACK-SILK - rev A - 2026-10-17 - ENGINEERING RELEASE



Assembly view

Key specifications

Interfaces	
Outline	10.09 x 10.00 mm
PCB	2 copper layers, 1.60 mm finished thickness
Fitted parts	2

Operating window

VIN supply voltage	12 V
Ambient operating temperature	0 to 70 °C

See Electrical limits for the conditions behind these values, required external loads and contact limits.

Electrical limits

Operating conditions and limits for the assembled board

Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply voltage	VIN	Required input supply voltage	12	–	12	V
Ambient operating temperature	TA	Ambient operating range	0	–	70	°C

Electrical characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
VIN supply current	IIN	[1, 2, 3]	0.5848	–	0.6157	mA
Power consumption	P	[4]	–	–	7.395	mW

How to use these limits

[1] Constant current during settled DC operation, drawn by the board itself.

[2] **Contacts:** What an attachment draws through a connector contact adds to this, up to that contact's limit.

[3] **Tolerances:** Calculated across the listed supply ranges and modeled component tolerances.

[4] Worst-case input power the board itself draws across all supply rails.

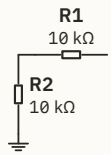
Use only the conditions printed with each value. Component absolute maximum ratings do not automatically apply to the assembled board.

Schematic

Passive network 10-BACK-SILK

KEY RAIL IN OUT BIDIR PASSIVE 5·p2 BLOCK 5, PAGE 2

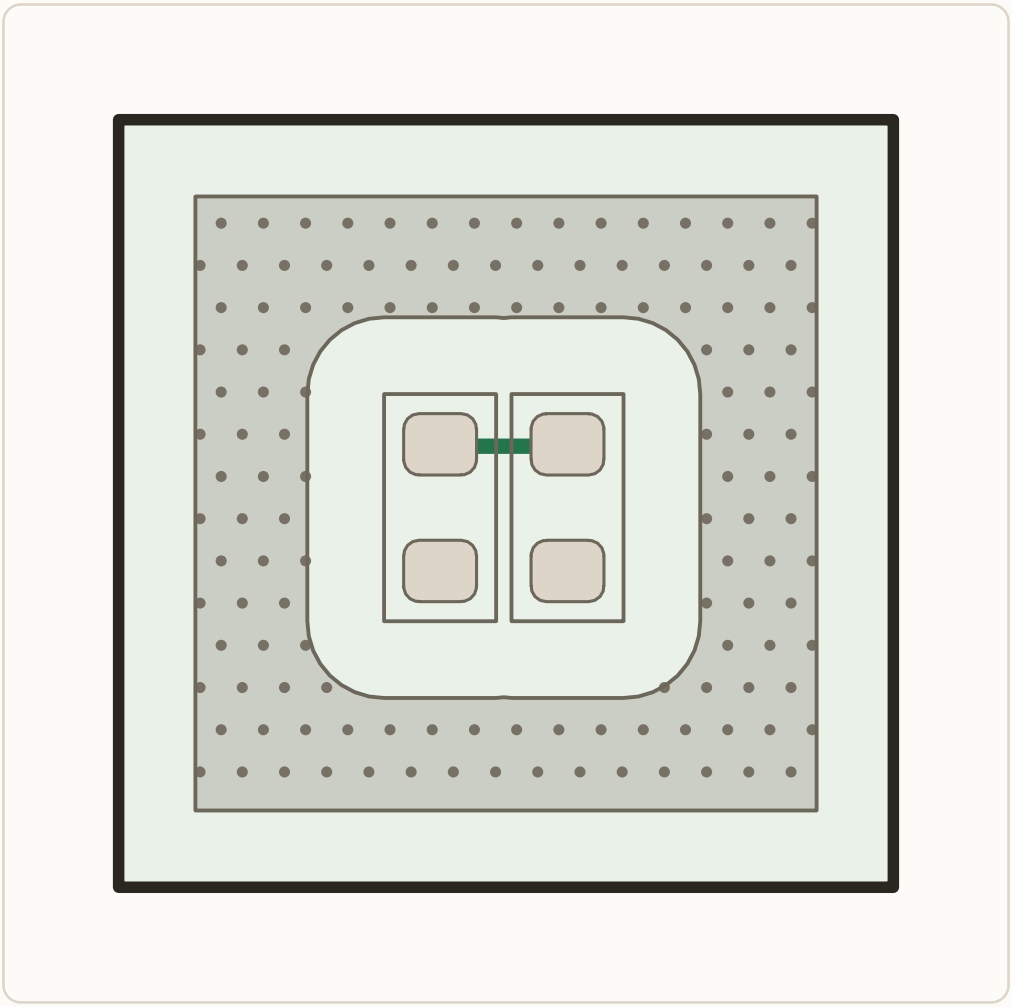
1 Passive network



Board layout

Copper on both layers, and the board area that no part or track uses

KEY — TOP COPPER — BOTTOM COPPER ▭ PAD ○ VIA



TOP VIEW · BOTTOM COPPER SEEN THROUGH · 10 X 10 MM · LARGE PARTS NAMED

Unused area

PATTERN	CAUSE	BOUNDED BY	AREA	OF BOARD
▭	**Edge margin**	between parts and the outline	**40.2 mm²**	**39.9 %**
	Total	at least 1 mm from everything	**40.2 mm²**	**39.9 %**

Unused area is board surface at least 1 mm from every part, track and the board edge. A part gap is the only kind a tighter placement can reclaim.

Components on this board

Component identities and supplier codes

IDENTIFICATION VIEWS ARE NOT TO SCALE

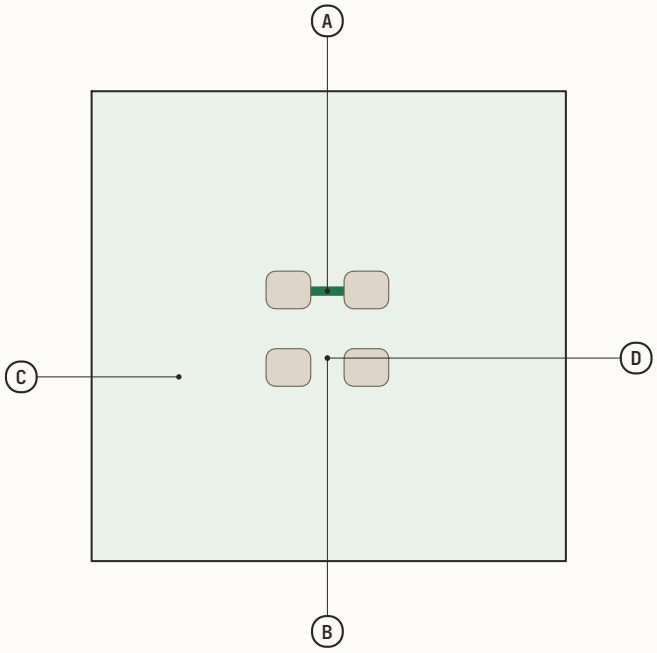
Passives

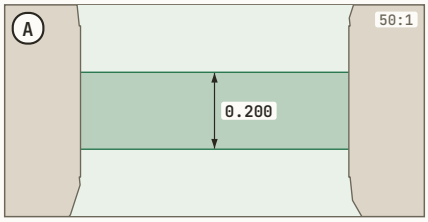
REFERENCE	VALUE / ROLE	QTY	PART
R1, R2	10k	2	C844918

Manufacturability

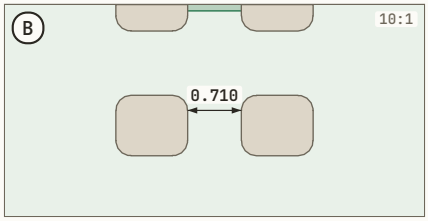
The smallest feature this board asks a fab to make, rule by rule

KEY — TOP COPPER — BOTTOM COPPER — PAD — MASK OPENING

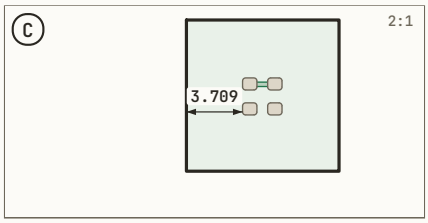




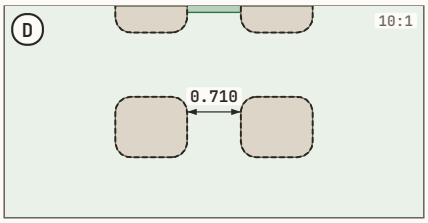
TRACK WIDTH
The one track segment
Required minimum 0.200; at minimum



COPPER TO COPPER, OUTER
Every outer gap between nets
Required minimum 0.1524; 0.558 above



COPPER TO EDGE
All copper, pours included
Required minimum 0.381; 3.328 above



MASK WEB
All 4 top mask openings
Required minimum 0.1016; 0.608 above

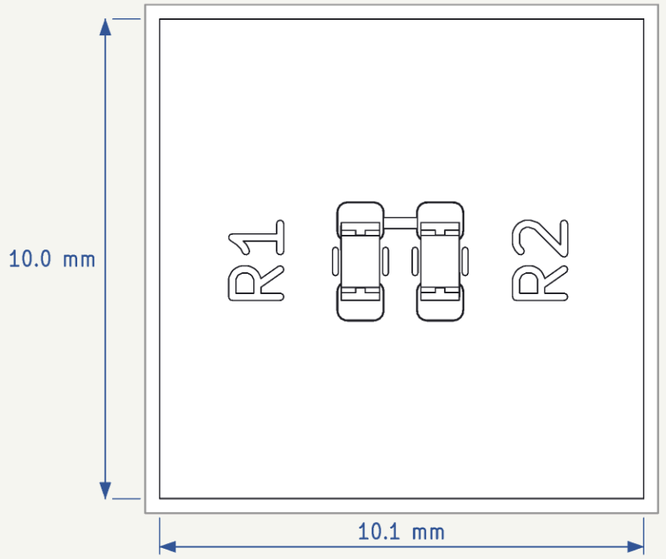
COMPATIBLE FABS

JLCPCB [1] — PCBWay [2] — OSH Park [3] — AISLER [4]

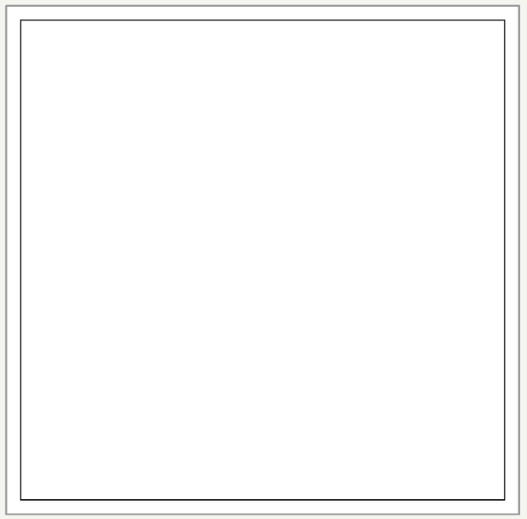
Detail minima use the strictest checked profile. Compatibility means the checked dimensional rules pass.

LAYERS	THICKNESS	HOLES	DRILL SIZES
2	1.6 mm		

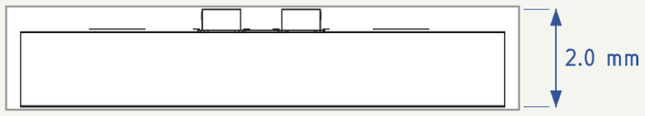
All values in mm. [1] read 2026-08-08 [2] read 2026-08-08 [3] read 2026-08-13 [4] read 2026-08-08



TOP VIEW



BOTTOM VIEW



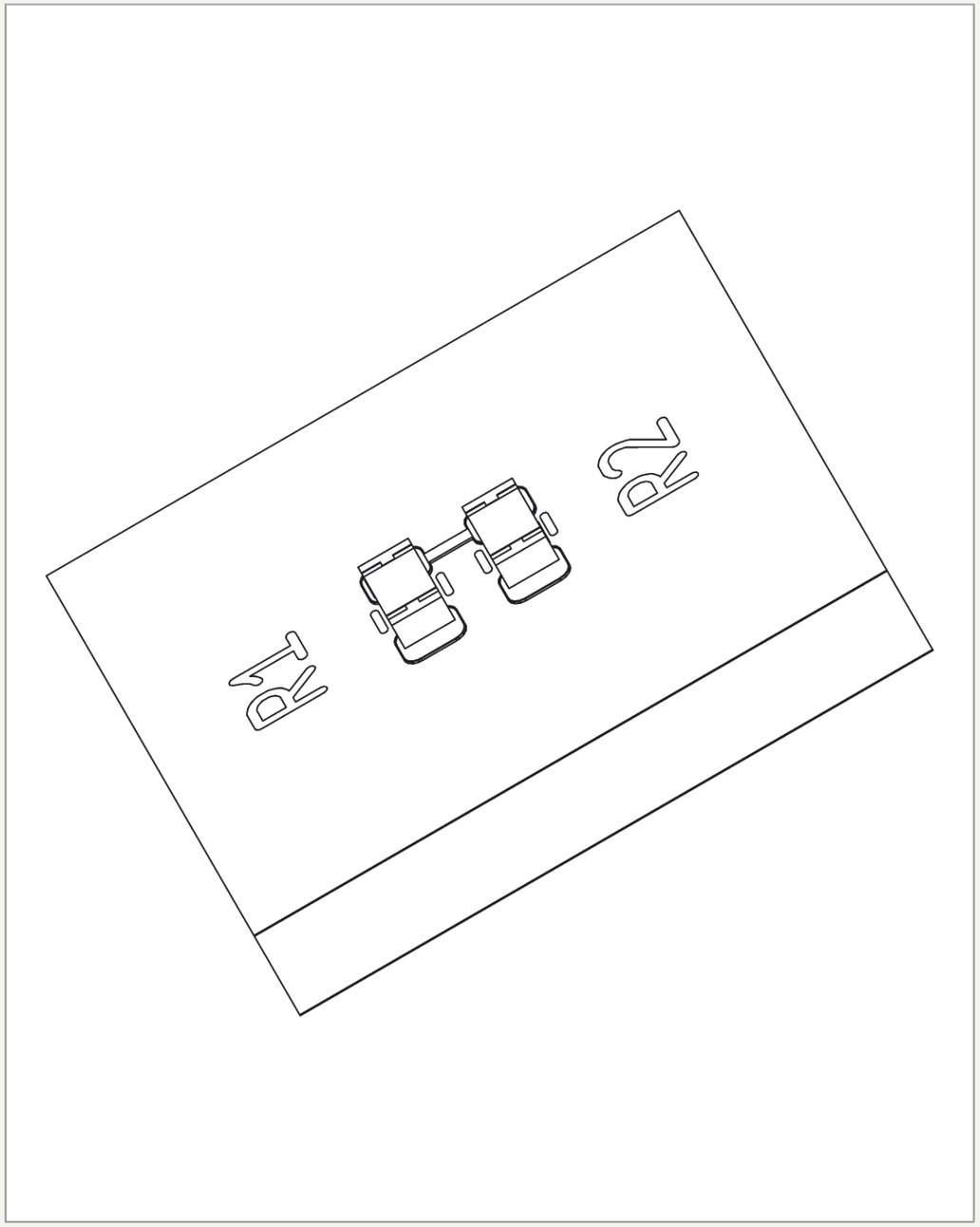
FRONT VIEW (Y)



LEFT VIEW (X)



RIGHT VIEW (X)



ISOMETRIC – NTS

TITLE 10 Back Silk assembly	DWG NO. 10–BACK–SILK
REV A	DATE 2026–10–17
OVERALL 10.1 x 10.0 x 2.0 mm	MATERIAL FR–4, 1.60 mm
PROJECTION REFERENCE VIEWS	SCALE NTS
UNITS mm	SHEET 1 OF 1