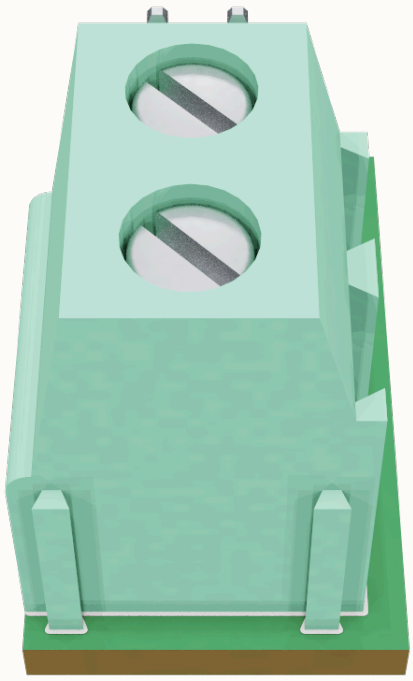
16 Edge Mate

16-EDGE-MATE - rev A - 2026-10-17 - ENGINEERING RELEASE



Assembly view

Key specifications

Interfaces	field harness in / daughterboard stack
Outline	11.30 x 19.72 mm
PCB	2 copper layers, 1.60 mm finished thickness
Fitted parts	4

Operating window

V12 supply voltage	**12 V**
Ambient operating temperature	**0 to 70 °C**

See Electrical limits for the conditions behind these values, required external loads and contact limits.

Connector overview

CONNECTOR	USE	SIGNALS
J1	field harness in	V12, GND
J2	daughterboard stack	V12, GND

Electrical limits

Operating conditions and limits for the assembled board

Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V12 supply voltage	V12	Required input supply voltage	12	—	12	V
Ambient operating temperature	TA	Ambient operating range	0	—	70	°C

Electrical characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V12 supply current	I12	[1, 2, 3]	0	—	1.848	mA
Power consumption	P	[4]	—	—	22.2	mW

Interface constraints

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
J1 current per contact	I(J1)	Pins 1, 2 [5]	—	—	2	mA
J2 current per contact	I(J2)	Pins 1, 2 [5]	—	—	2	mA

How to use these limits

[1] Maximum instantaneous current in the modeled window, drawn by the board itself.

[2] **Contacts:** What an attachment draws through a connector contact adds to this, up to that contact's limit.

[3] **Tolerances:** Calculated across the listed supply ranges and modeled component tolerances.

[4] Worst-case input power the board itself draws across all supply rails.

[5] **Contact current:** Each listed pin must not exceed this current. These are application design limits, not connector ratings or available output current.

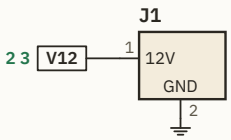
Use only the conditions printed with each value. Component absolute maximum ratings do not automatically apply to the assembled board.

Schematic

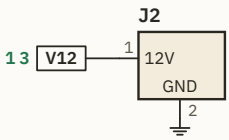
Terminal, header and V12 input 16-EDGE-MATE

KEY RAIL IN OUT BIDIR PASSIVE 5·p2 BLOCK 5, PAGE 2

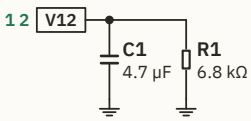
1 Terminal



2 Header



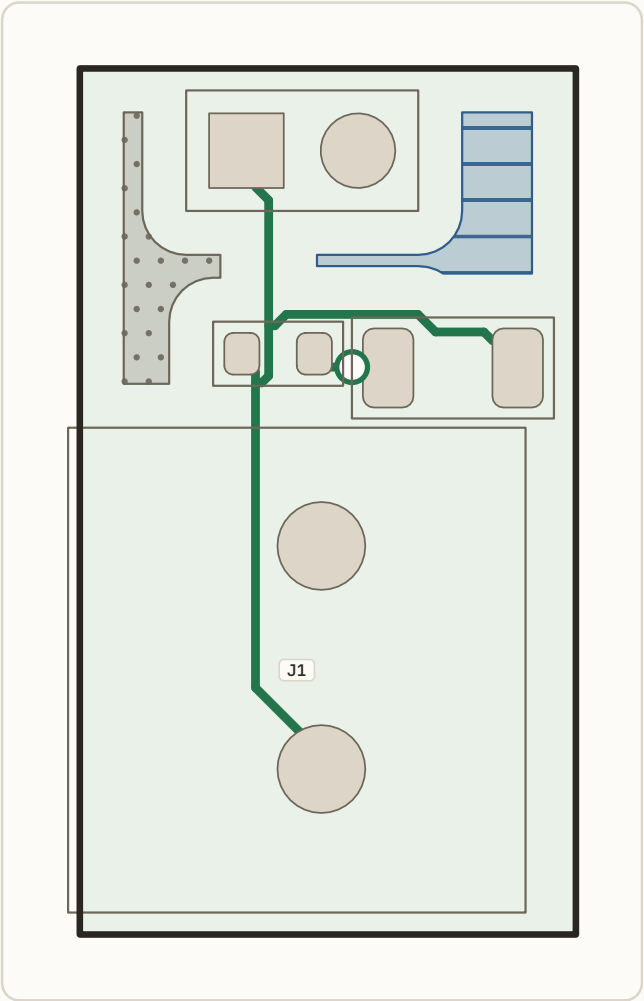
3 V12 input



Board layout

Copper on both layers, and the board area that no part or track uses

KEY — TOP COPPER — BOTTOM COPPER PAD VIA



TOP VIEW · BOTTOM COPPER SEEN THROUGH · 11 X 20 MM · LARGE PARTS NAMED

Unused area

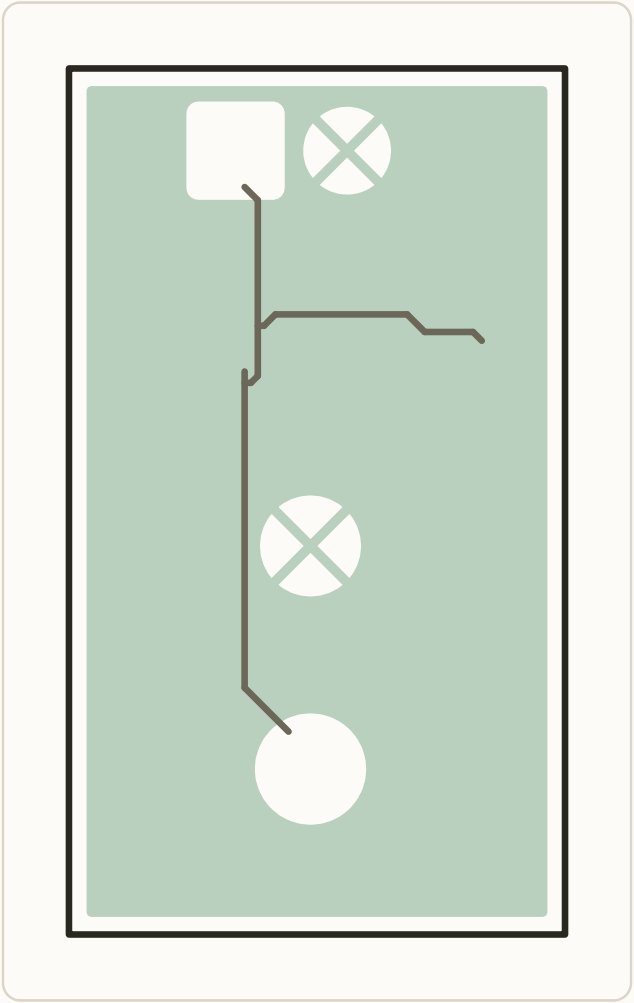
PATTERN	CAUSE	BOUNDED BY	AREA	OF BOARD
	Connector apron	beside a connector	7.0 mm²	3.1 %
	Edge margin	between parts and the outline	5.5 mm²	2.4 %
	Total	at least 1 mm from everything	12.5 mm²	5.6 %

Unused area is board surface at least 1 mm from every part, track and the board edge. A part gap is the only kind a tighter placement can reclaim.

Ground plane

Ground on B.Cu under the routes on F.Cu

KEY GROUND PLANE OPENING ROUTE ON F.CU



TOP VIEW · B.CU UNDER F.CU

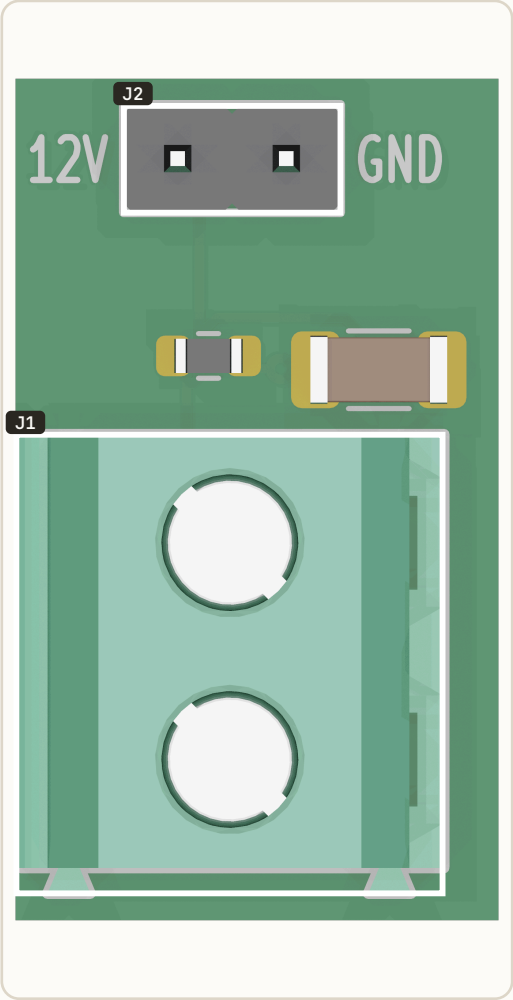
Return path

Ground plane	B.Cu, 82 % of the board
Routes on F.Cu	19 mm; no return detour of 1 mm or more

Openings in the plane add under 1 mm to the return path of a route on F.Cu above them; no route on F.Cu crosses a gap that adds more.

Board connections

Connector and test point locations viewed from the top of the assembled board



TOP VIEW - CONNECTORS AND TEST POINTS MARKED - NOT TO SCALE

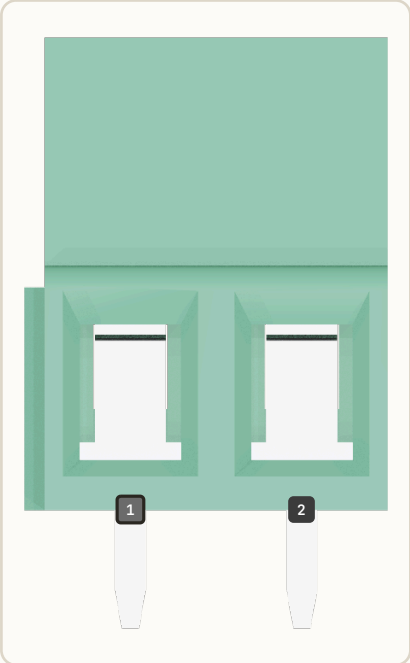
Pin schedules and mating-face views are on the following pages.

Connector pinout

Pin numbers are shown as viewed into the mating face

SIGNAL CLASS SIGNAL GROUND

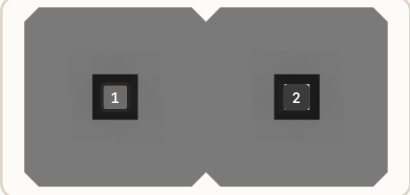
J1 - field harness in



MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	V12	V12 signal
2	GND	Ground reference

J2 - daughterboard stack



TOP MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	V12	V12 signal
2	GND	Ground reference

Components on this board

Component identities and supplier codes

IDENTIFICATION VIEWS ARE NOT TO SCALE



C8465
field harness in
J1 · QTY 1 · LCSC C8465



C492401
daughterboard stack
J2 · QTY 1 · LCSC C492401

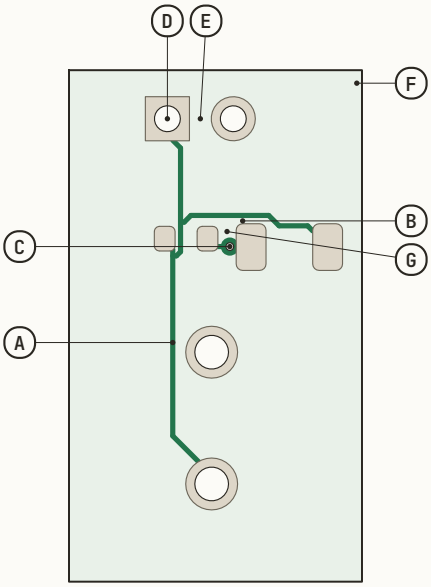
Passives

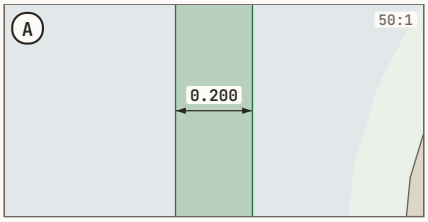
REFERENCE	VALUE / ROLE	QTY	PART
C1	entry bulk	1	C440156
R1	C1 bleeder	1	C2907055

Manufacturability

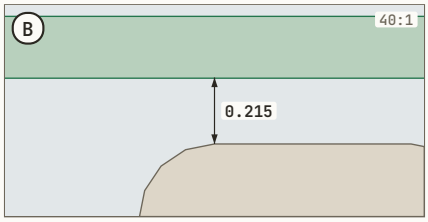
The smallest feature this board asks a fab to make, rule by rule

KEY — TOP COPPER — BOTTOM COPPER — PAD — MASK OPENING

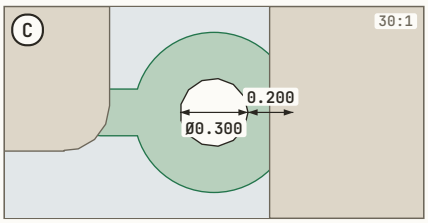




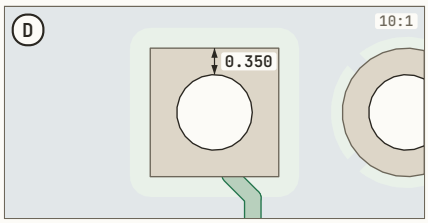
TRACK WIDTH
All 14 track segments
Required minimum 0.200; at minimum



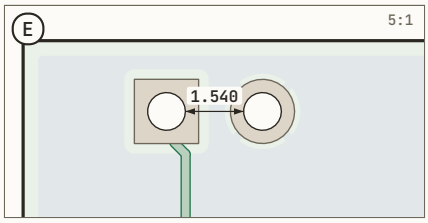
COPPER TO COPPER, OUTER
Every outer gap between nets
Required minimum 0.1524; 0.062 above



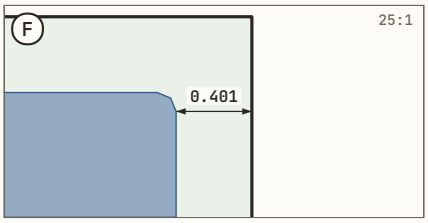
FINISHED DRILL · VIA RING
All 5 holes; the one via
Finished drill minimum 0.300; at minimum.
Via ring minimum 0.200; at minimum



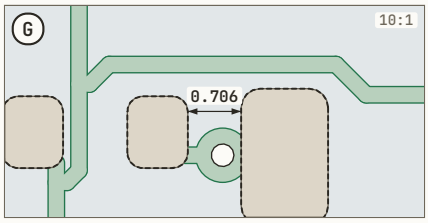
PTH RING
All 4 plated leads
Required minimum 0.300; 0.050 above



HOLE TO HOLE
All 5 holes, wall to wall
Required minimum 0.300; 1.240 above



COPPER TO EDGE
All copper, pours included
Required minimum 0.381; 0.020 above



MASK WEB
All 8 top mask openings
Required minimum 0.1016; 0.604 above

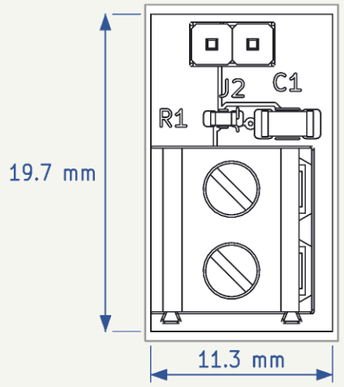
COMPATIBLE FABS

JLCPCB [1] · PCBWay [2] · OSH Park [3] · AISLER [4]

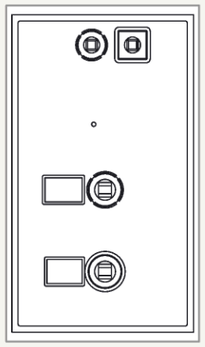
Detail minima use the strictest checked profile. Compatibility means the checked dimensional rules pass.

LAYERS	THICKNESS	ASPECT RATIO	HOLES	DRILL SIZES
2	1.6 mm	5.3 : 1	1 via, 4 PTH	3, Ø0.300–1.300

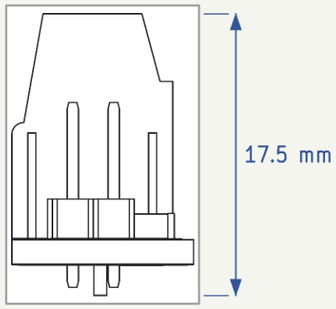
All values in mm. [1] read 2026-08-08 [2] read 2026-08-08 [3] read 2026-08-13 [4] read 2026-08-08



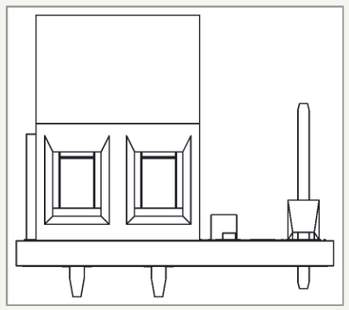
TOP VIEW



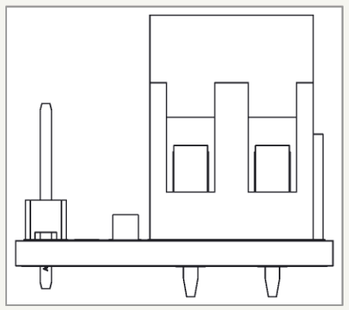
BOTTOM VIEW



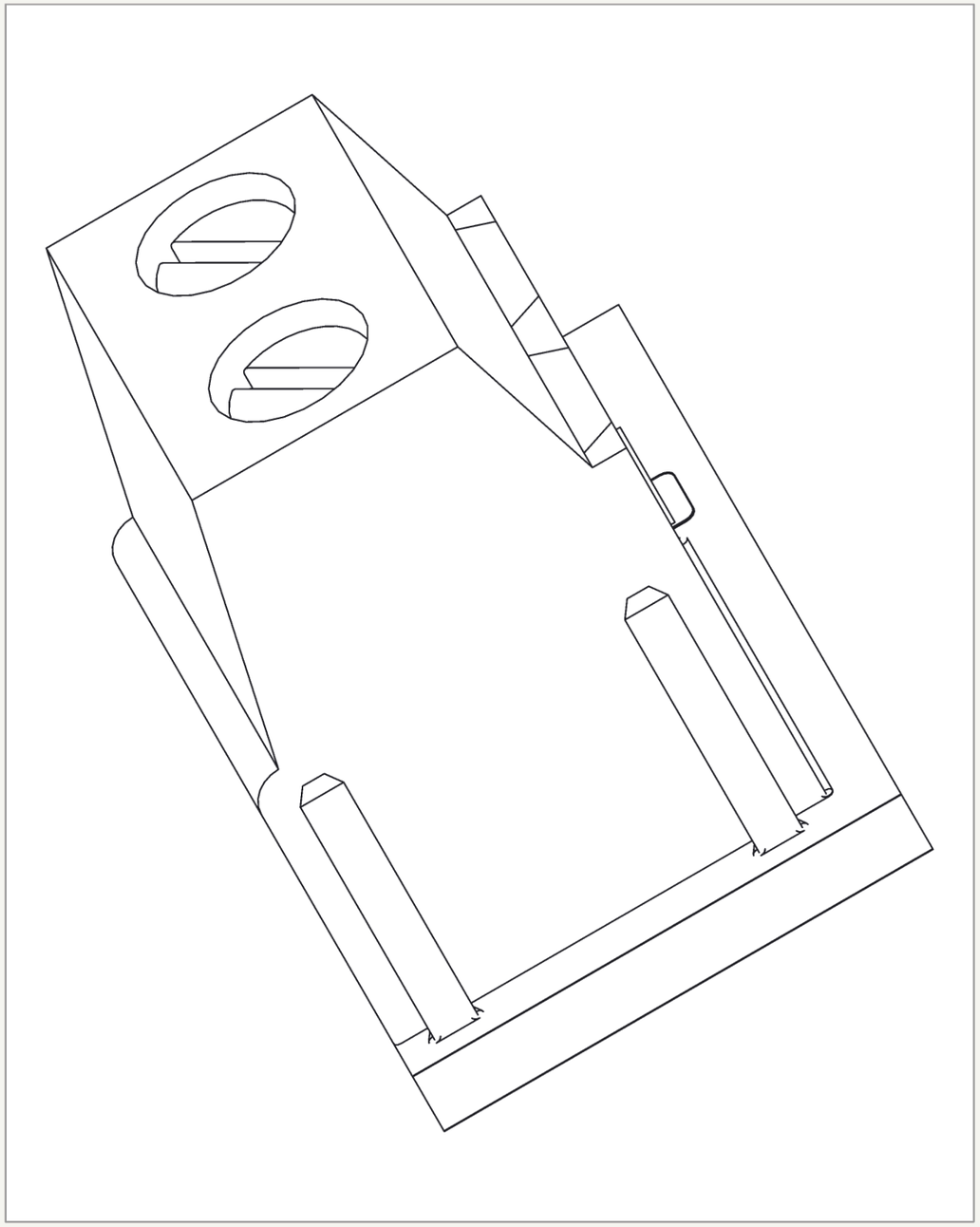
FRONT VIEW (Y)



LEFT VIEW (X)



RIGHT VIEW (X)



ISOMETRIC – NTS

TITLE 16 Edge Mate assembly	DWG NO. 16–EDGE–MATE
REV A	DATE 2026–10–17
OVERALL 11.3 x 19.7 x 17.5 mm	MATERIAL FR–4, 1.60 mm
PROJECTION REFERENCE VIEWS	SCALE NTS
UNITS mm	SHEET 1 OF 1