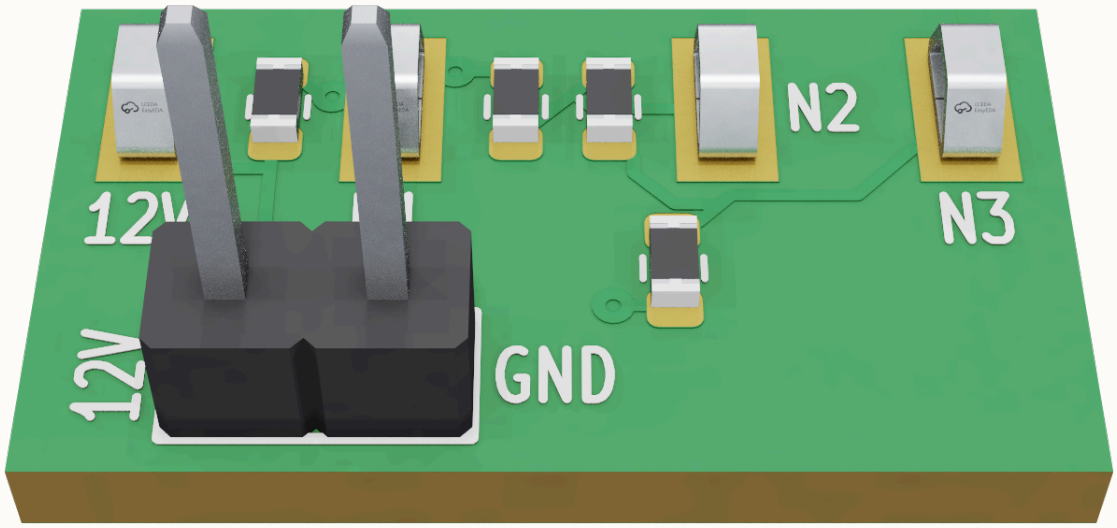
17 Align

17-ALIGN - rev A - 2026-10-17 - ENGINEERING RELEASE



Assembly view

Key specifications

Interfaces	field power in
Outline	17.77 x 10.20 mm
PCB	2 copper layers, 1.60 mm finished thickness
Fitted parts	9

Operating window

V12 supply voltage	**12 V**
Ambient operating temperature	**0 to 70 °C**

See Electrical limits for the conditions behind these values, required external loads and contact limits.

Connector overview

CONNECTOR	USE	SIGNALS
J1	field power in	V12, GND

Electrical limits

Operating conditions and limits for the assembled board

Recommended operating conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V12 supply voltage	V12	Required input supply voltage	12	—	12	V
Ambient operating temperature	TA	Ambient operating range	0	—	70	°C

Electrical characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
V12 supply current	I12	[1, 2, 3]	0.2921	—	0.3082	mA
Power consumption	P	[4]	—	—	3.702	mW

How to use these limits

[1] Constant current during settled DC operation, drawn by the board itself.

[2] **Contacts:** What an attachment draws through a connector contact adds to this, up to that contact's limit.

[3] **Tolerances:** Calculated across the listed supply ranges and modeled component tolerances.

[4] Worst-case input power the board itself draws across all supply rails.

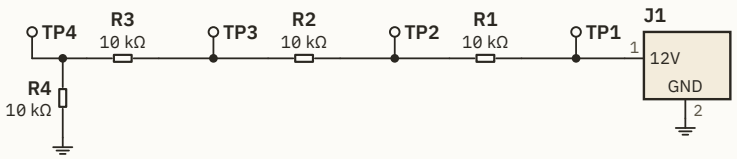
Use only the conditions printed with each value. Component absolute maximum ratings do not automatically apply to the assembled board.

Schematic

Header 17-ALIGN

KEY RAIL IN OUT BIDIR PASSIVE 5·p2 BLOCK 5, PAGE 2

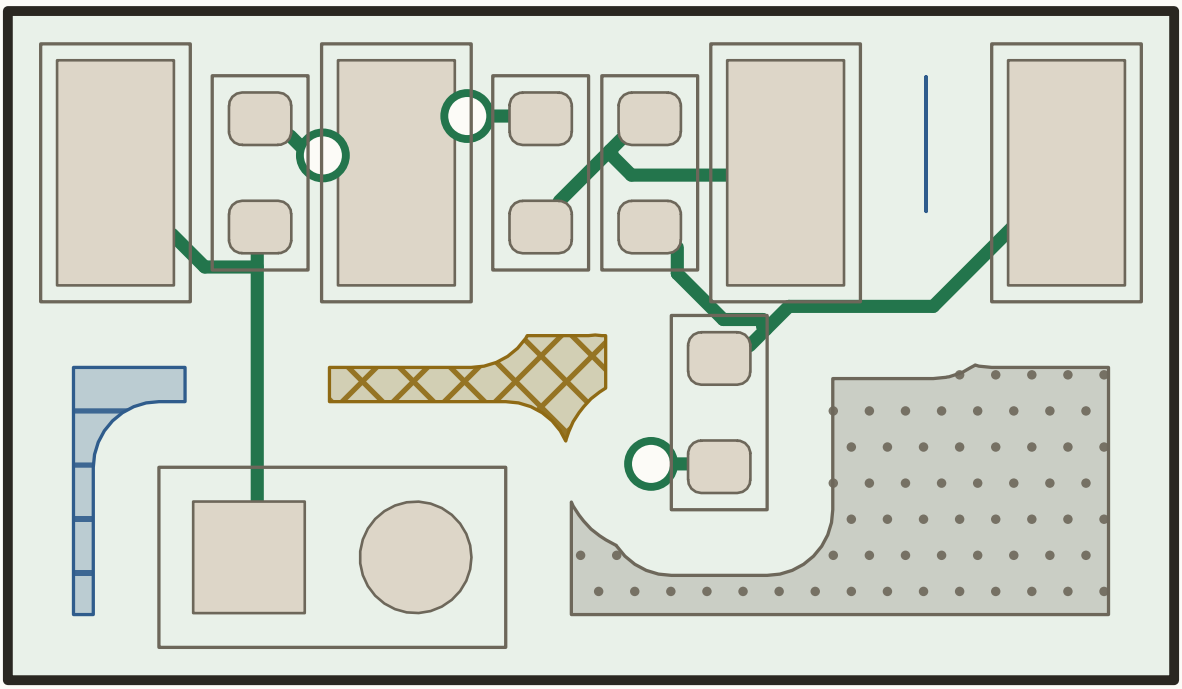
1 Header



Board layout

Copper on both layers, and the board area that no part or track uses

KEY — TOP COPPER — BOTTOM COPPER PAD VIA



TOP VIEW · BOTTOM COPPER SEEN THROUGH · 18 X 10 MM · LARGE PARTS NAMED

Unused area

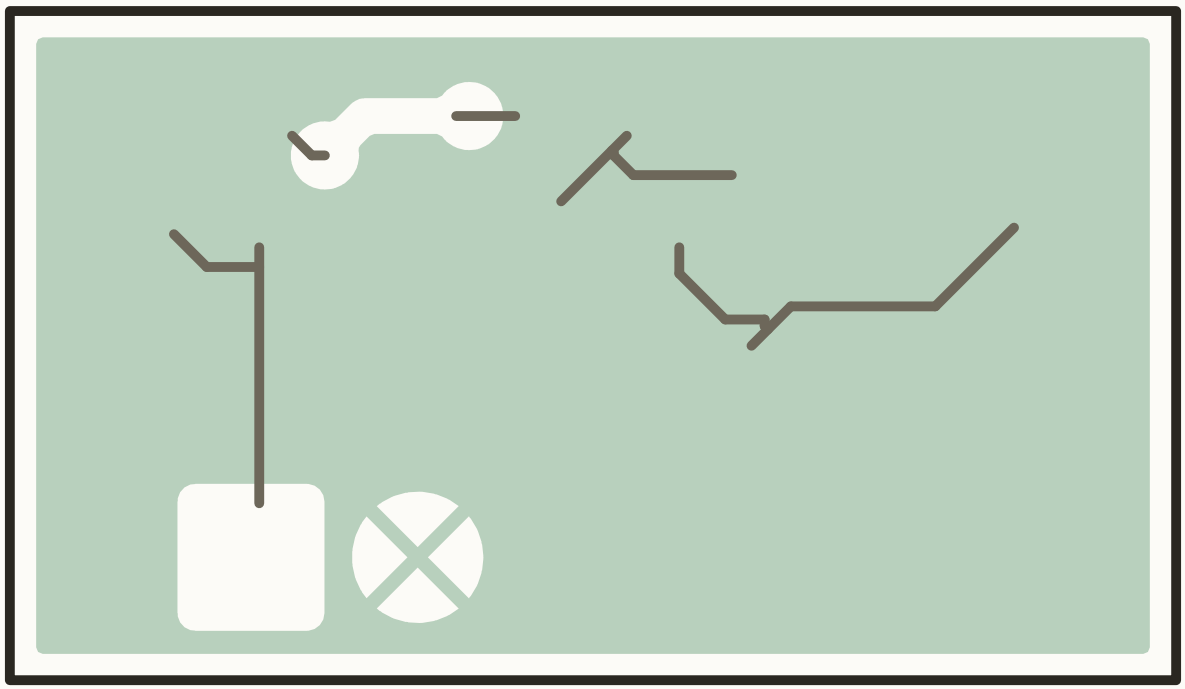
PATTERN	CAUSE	BOUNDED BY	AREA	OF BOARD
	Part gap	between parts	3.1 mm²	1.7 %
	Connector apron	beside a connector	2.1 mm²	1.2 %
	Edge margin	between parts and the outline	18.7 mm²	10.3 %
	Total	at least 1 mm from everything	23.9 mm²	13.2 %

Unused area is board surface at least 1 mm from every part, track and the board edge. A part gap is the only kind a tighter placement can reclaim.

Ground plane

Ground on B.Cu under the routes on F.Cu

KEY GROUND PLANE OPENING ROUTE ON F.CU



TOP VIEW · B.CU UNDER F.CU

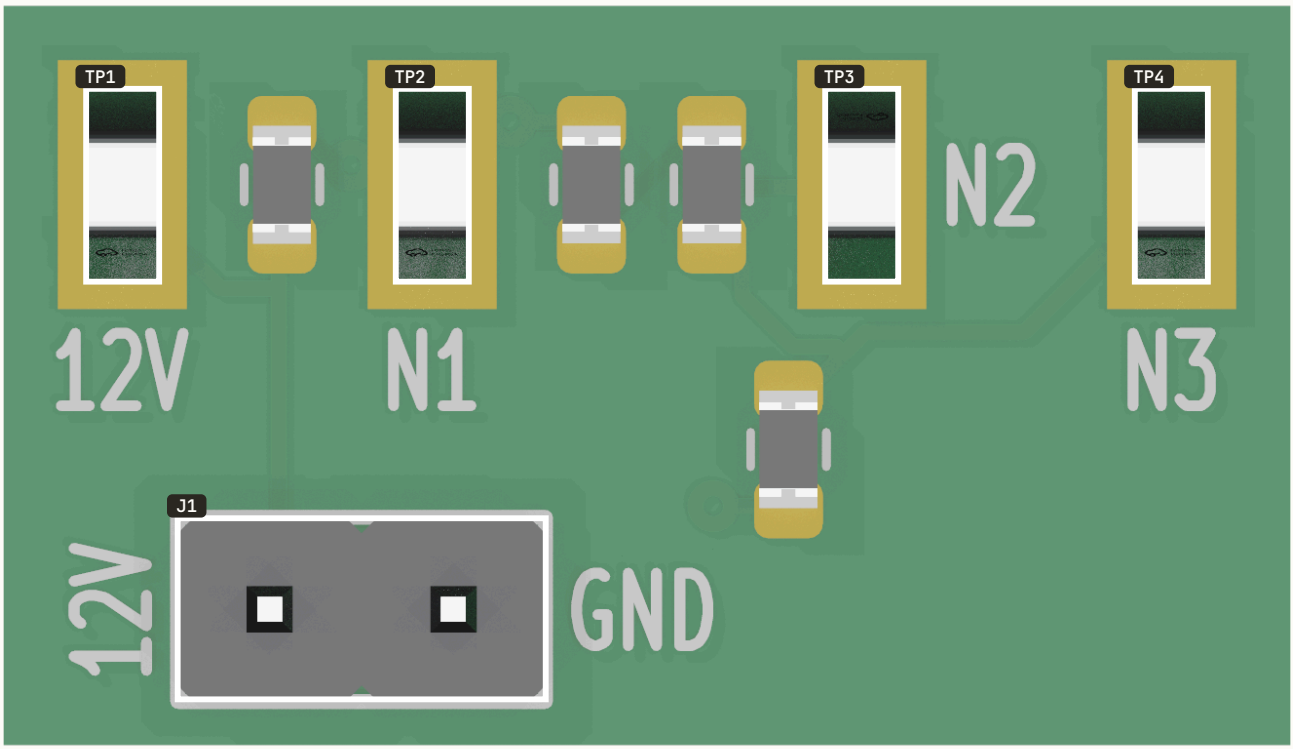
Return path

Ground plane	B.Cu, 83 % of the board
Routes on F.Cu	17 mm; no return detour of 1 mm or more

Openings in the plane add under 1 mm to the return path of a route on F.Cu above them; no route on F.Cu crosses a gap that adds more.

Board connections

Connector and test point locations viewed from the top of the assembled board



TOP VIEW - CONNECTORS AND TEST POINTS MARKED - NOT TO SCALE

Test point locations

STATION	SIGNAL	PINS	CONNECTED TO
TP1	V12	1	to J1, R1
TP2	N1	1	to R1, R2
TP3	N2	1	to R2, R3
TP4	N3	1	to R3, R4

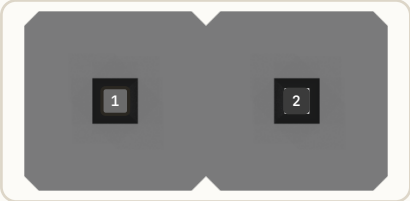
Pin schedules and mating-face views are on the following pages.

Connector pinout

Pin numbers are shown as viewed into the mating face

SIGNAL CLASS SIGNAL GROUND

J1 - field power in



TOP MATING FACE VIEW

PIN	SIGNAL	DESCRIPTION
1	V12	V12 signal
2	GND	Ground reference

Components on this board

Component identities and supplier codes

IDENTIFICATION VIEWS ARE NOT TO SCALE



C492401
field power in
J1 · QTY 1 · LCSC C492401



C2906768
probe 12V
TP1 · QTY 1 · LCSC C2906768



C2906768
probe N1
TP2 · QTY 1 · LCSC C2906768



C2906768
probe N2
TP3 · QTY 1 · LCSC C2906768



C2906768
probe N3
TP4 · QTY 1 · LCSC C2906768

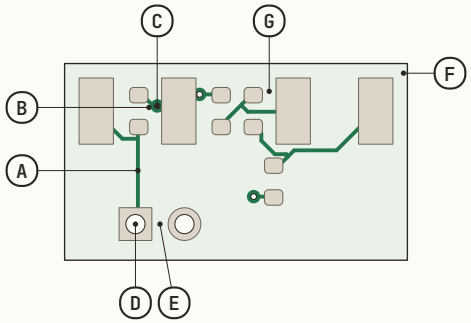
Passives

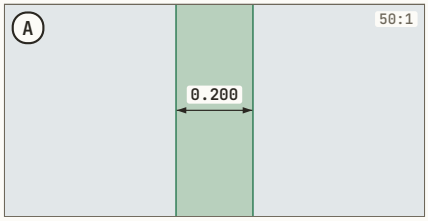
REFERENCE	VALUE / ROLE	QTY	PART
R1	ladder 1	1	C844918
R2	ladder 2	1	C844918
R3	ladder 3	1	C844918
R4	ladder 4	1	C844918

Manufacturability

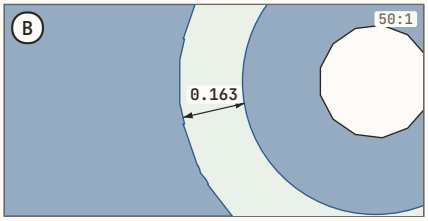
The smallest feature this board asks a fab to make, rule by rule

KEY — TOP COPPER — BOTTOM COPPER — PAD — MASK OPENING

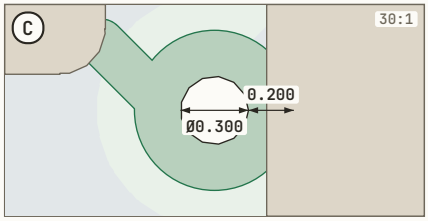




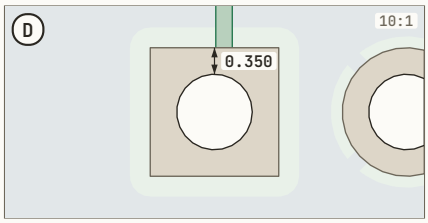
TRACK WIDTH
All 22 track segments
Required minimum 0.200; at minimum



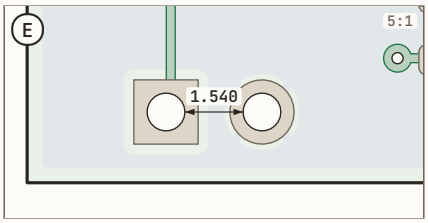
COPPER TO COPPER, OUTER
Every outer gap between nets
Required minimum 0.1524; 0.011 above



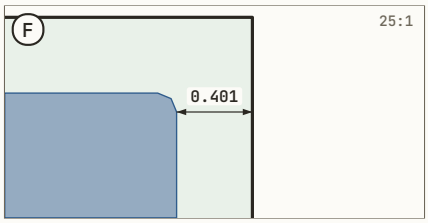
FINISHED DRILL · VIA RING
All 5 holes; all 3 vias
Finished drill minimum 0.300; at minimum.
Via ring minimum 0.200; at minimum



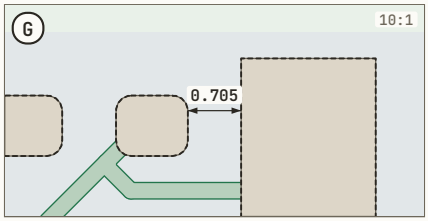
PTH RING
All 2 plated leads
Required minimum 0.300; 0.050 above



HOLE TO HOLE
All 5 holes, wall to wall
Required minimum 0.300; 1.240 above



COPPER TO EDGE
All copper, pours included
Required minimum 0.381; 0.020 above



MASK WEB
All 14 top mask openings
Required minimum 0.1016; 0.604 above

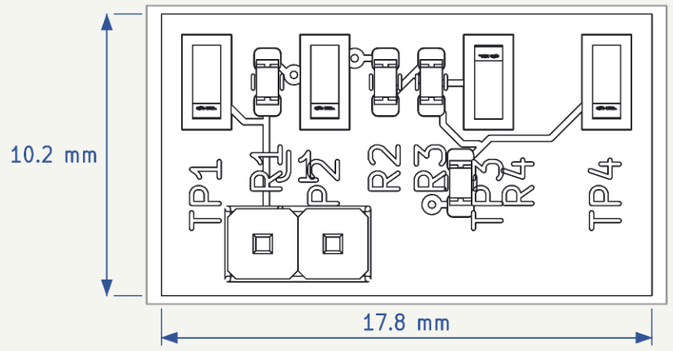
COMPATIBLE FABS

JLCPCB [1] — PCBWay [2] — OSH Park [3] — AISLER [4]

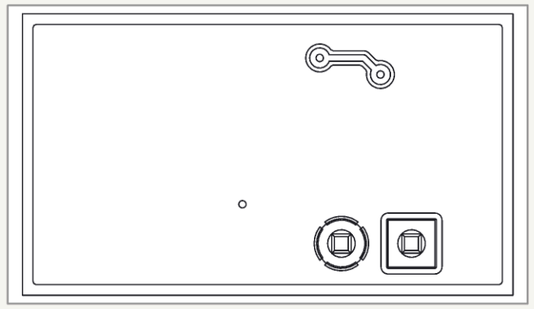
Detail minima use the strictest checked profile. Compatibility means the checked dimensional rules pass.

LAYERS	THICKNESS	ASPECT RATIO	HOLES	DRILL SIZES
2	1.6 mm	5.3 : 1	3 via, 2 PTH	2, Ø0.300–1.000

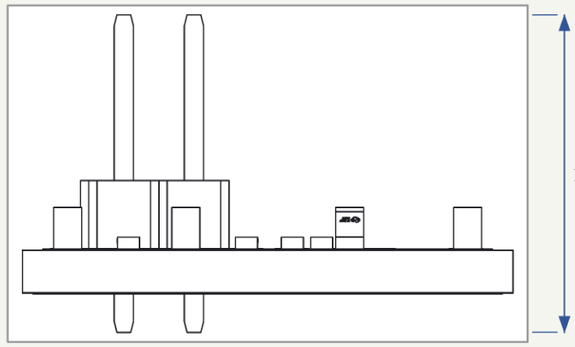
All values in mm. [1] read 2026-08-08 [2] read 2026-08-08 [3] read 2026-08-13 [4] read 2026-08-08



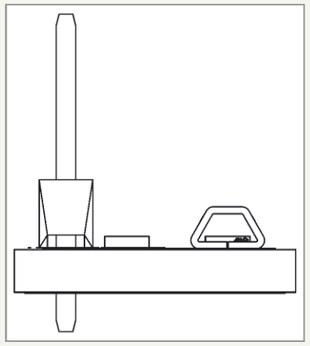
TOP VIEW



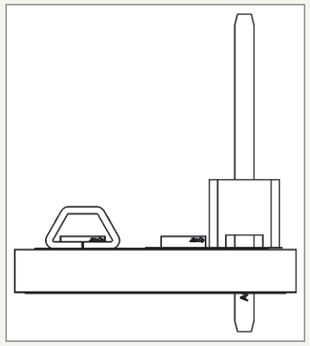
BOTTOM VIEW



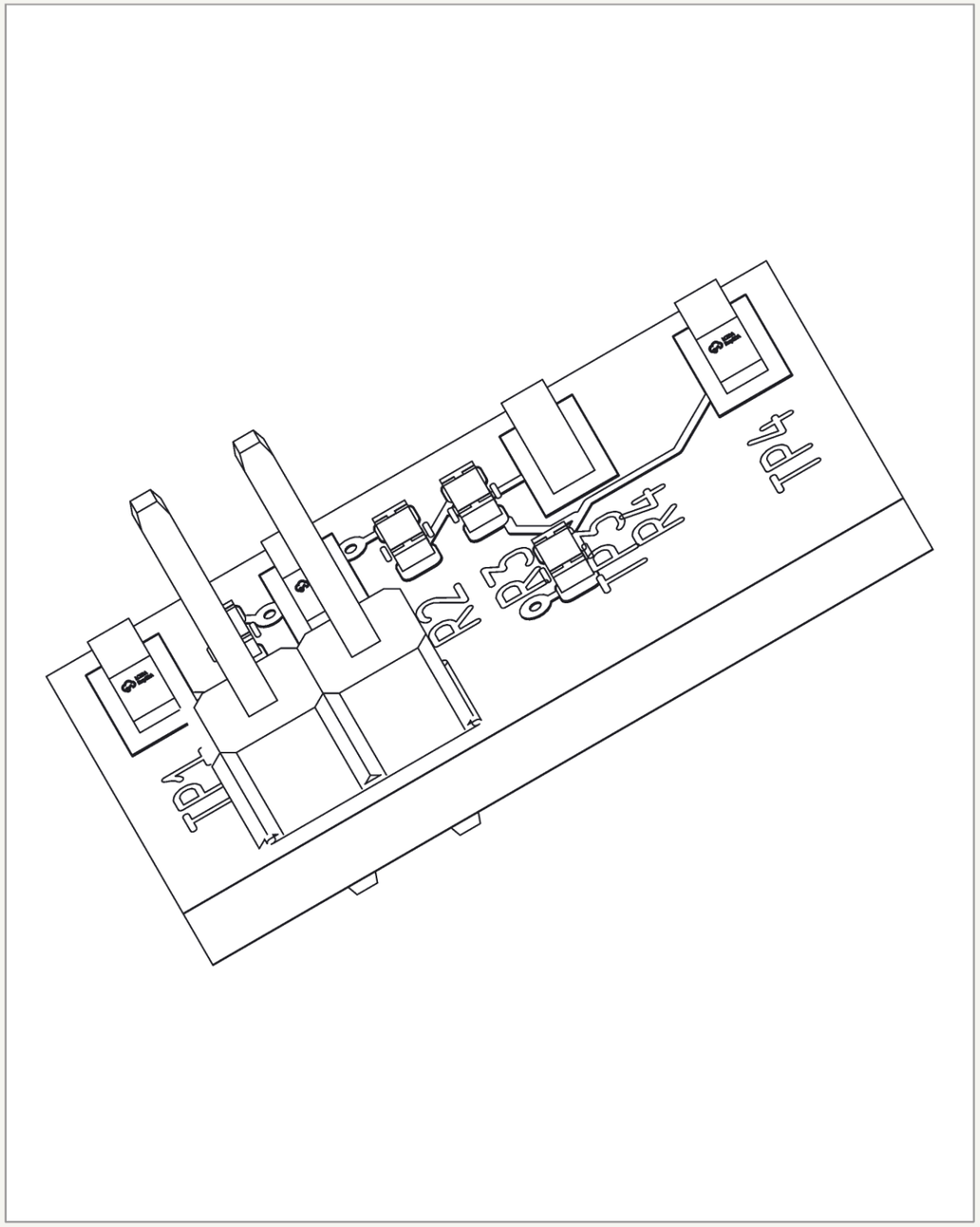
FRONT VIEW (Y)



LEFT VIEW (X)



RIGHT VIEW (X)



ISOMETRIC – NTS

TITLE 17 Align assembly	DWG NO. 17–ALIGN
REV A	DATE 2026–10–17
OVERALL 17.8 x 10.2 x 11.5 mm	MATERIAL FR–4, 1.60 mm
PROJECTION REFERENCE VIEWS	SCALE NTS
UNITS mm	SHEET 1 OF 1